Standard Products

UT200SpW4RTR-EVB 4-Port SpaceWire Router Evaluation Board Users Guide

User Manual
November, 2010
www.aeroflex.com/spacewire

1.0 INTRODUCTION

The UT200SpW4RTR-EVB is a 4-Port SpaceWire Router evaluation board designed to allow the system designer access to all the features of the UT200SpW4RTR 4-Port router as defined in the datasheet (www.aeroflex.com/spacewire). The 4-Port router is capable of operating at data rates from 10 to 200 Mbps. A parallel host interface is accessible through an onboard FPGA. The Evaluation board can also be plugged into the Aeroflex Gaisler LEON 3-FT evaluation board, further expanding functionality of the UT200SpW4RTR-EVB.

The UT200SpW4RTR router implements a non-blocking crosspoint switch and a "Round Robin" arbitration scheme allowing all five receive ports access to all five transmit ports. Path and logical addressing are supported (Per ECSS-E-ST-50- 12C) and lookup table storage is replicated five times giving each receive port a dedicated block of memory for logical addressing. Configuration of lookup tables, as well as, access to internal registers may occur through any of the five ports using a simple configuration protocol. A group adaptive function is also provided for two ports when implementing logical addressing.

Each of the four SpaceWire ports is capable of running at an independent speed. The clocking of the 4-port router is provided by Aeroflex's Clock Network Manager II. This allows the users systems to be configured with nodes/instruments running at different speeds.

2.0 SCOPE

This document describes the features and necessary steps to set-up and operate the Aeroflex SpaceWire 4-port Router Evaluation Board. It is recommended that the user be familiar with the UT200SpW4RTR 4-Port SpaceWire Router datasheet.

3.0 REFERENCE DOCUMENTS

ESA Publications Division, "SpaceWire Standard: ECSS-E-ST-50-12C", http://www.ecss.nl/.

Aeroflex, "UT200SpW4RTR Datasheet", www.aeroflex.com

Aeroflex, "UT7R2XLR816 Datasheet", www.aeroflex.com

Aeroflex, "UT54LVDS031LV Datasheet", www.aeroflex.com

Aeroflex, "UT54LVDS032LV Datasheet", www.aeroflex.com

Aeroflex Gaisler GR-CPCI-UT699 LEON3-FT CPCI Development Board, www.gaisler.com

4.0 FUNCTIONAL DIAGRAM

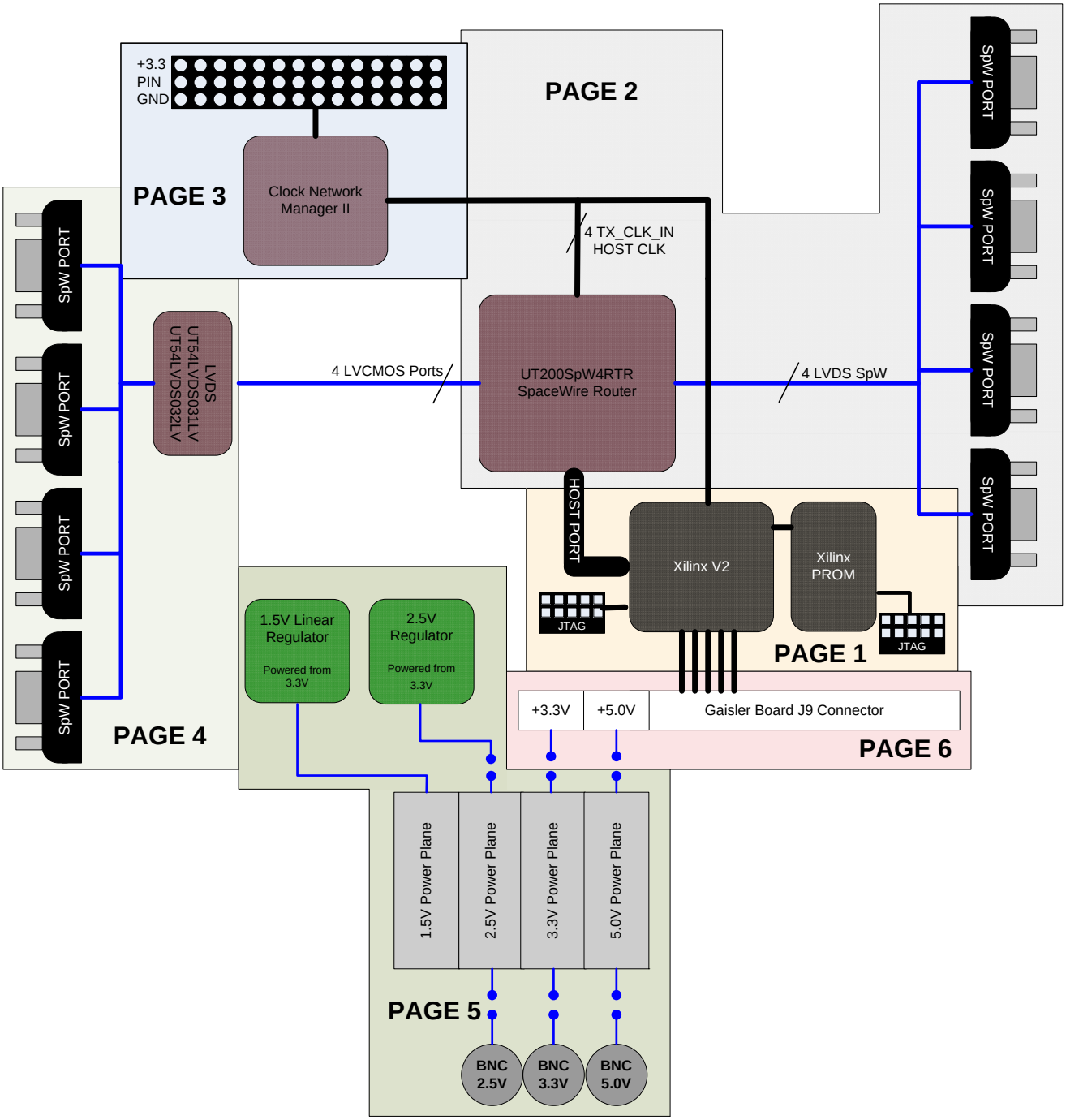

Figure 1. Notional UT200SpW4RTR-EVB block diagram

5.0 FEATURES AND GENERAL OPERATION

The Aeroflex 4-Port SpaceWire Router evaluation board is designed to provide the user a flexible means to configure, control, access, and route data through the UT200SpW4RTR device. Power to the board may be provided through the J9 connector on the GR-UT699 CPCI Development Board or through the BNC connectors. Only one power source should be used at a time.

Clocking of the board is done via the UT7R2XLR816 Clock Network Manager. The UT7R2XLR816 can be configured using the on board FPGA (Xilinx V2) or using the designated jumpers. The user is encouraged to download the UT7R2XLR816 Clock Network Manager Software GUI available at www.aeroflex.com/clocks and familiarize themselves with the UT7R2XLR816 Clock Network Manager datasheet.

The 4-Port router device can be accessed using any of the four SpaceWire ports or through the V2 FPGA that is connected to the Host port of the router. The FPGA on the board can be controlled and programmed by using either the JTAG connector or using the LEON 3FT on the GR-UT699 Evaluation board. All of these features are detailed in the following sections.

5.1 Power

5.1.1 External Power

Power to the UT200SpW4RTR-EVB may be provided externally using the three BNC connectors. 5.0V, 3.3V and 2.5V must be provided to the board. In order to use external power provided by the BNC connectors the user must jumper J57, J58, and J59. These jumpers ensure that external power is flowing to the board. Ensure that Jumpers J64 and J65 are removed!

To avoid large surge currents in the UT200SpW4RTR device, VDD = 3.3V (J57) should be powered up either before VDDC = 2.5V (J59) or synchronously with VDDC (VDD > VDDC). DO NOT power up the core voltage supply VDDC before the I/O supply VDD; doing so causes a large in-rush current from VDDC to VDD that stresses the power supplies and router components. If VDD and VDDC are being powered up synchronously ensure that the voltage difference between VDDC and VDD does not exceed 0.4V (VDDC - VDD < 0.4V). See AC Electrical Characteristics in the UT200SpW4RTR datasheet for specifics.

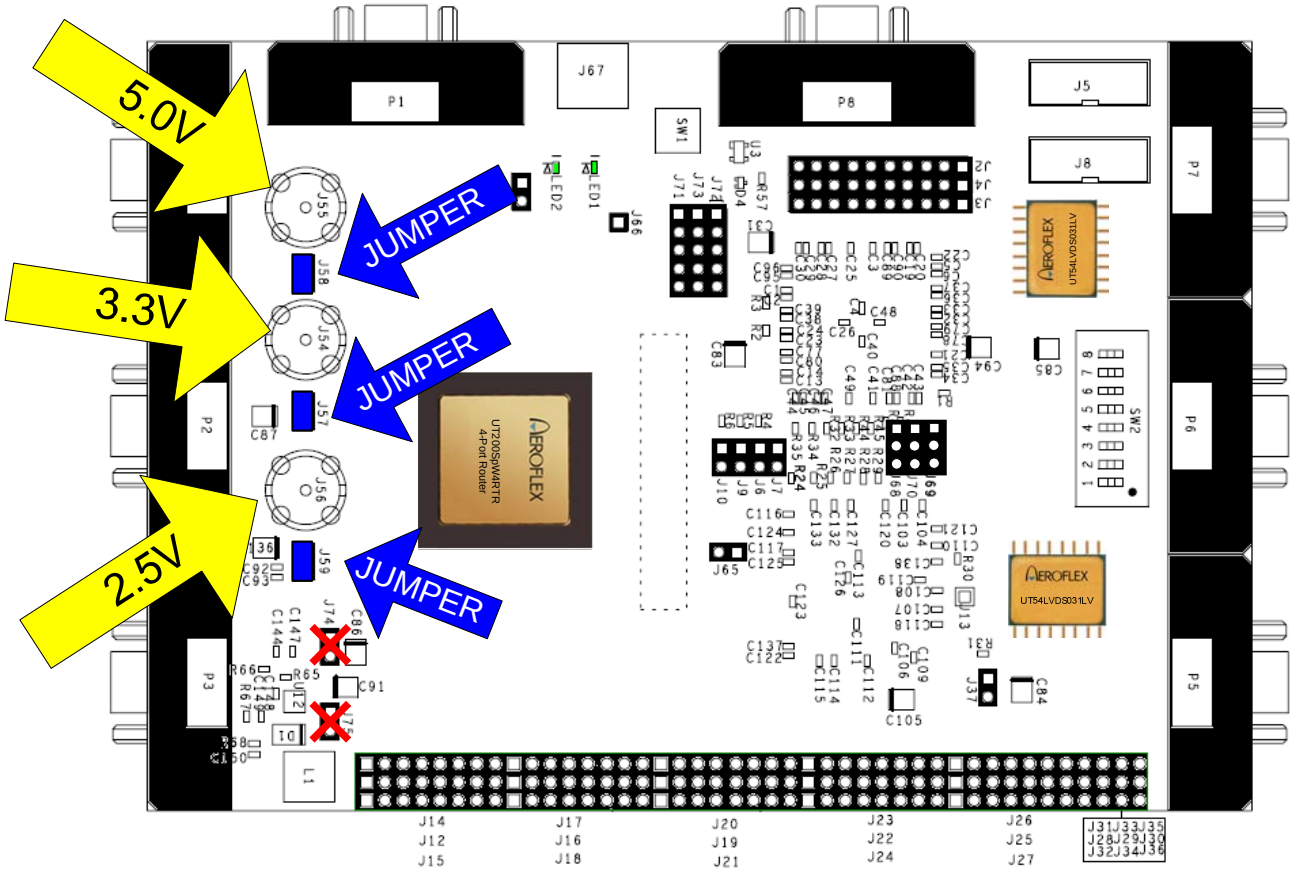

Figure 2. External Power Jumper Configuration Settings

5.1.2 Aeroflex Gaisler Board Power

Power to the UT200SpW4RTR-EVB may also be provided from the J9 connector on the GR-CPCI-UT699 LEON3-FT CPCI Development Board. Jumpers J64 and J65 must be set in order for the 120 pin J63 connector on the 4-Port EVB to receive power from the LEON-3FT board. J63, the 120 pin connector, is located on the back side of the UT200SpW4RTR-EVB. Use caution when mating the UT200SpW4RTR-EVB to the LEON-3FT evaluation board. If the UT200SpW4RTR-EVB will be receiving power from the UT699 Evaluation board, jumpers J57, J58, and J59 should be removed.

NOTE: Only connect jumpers required for the power source in use.

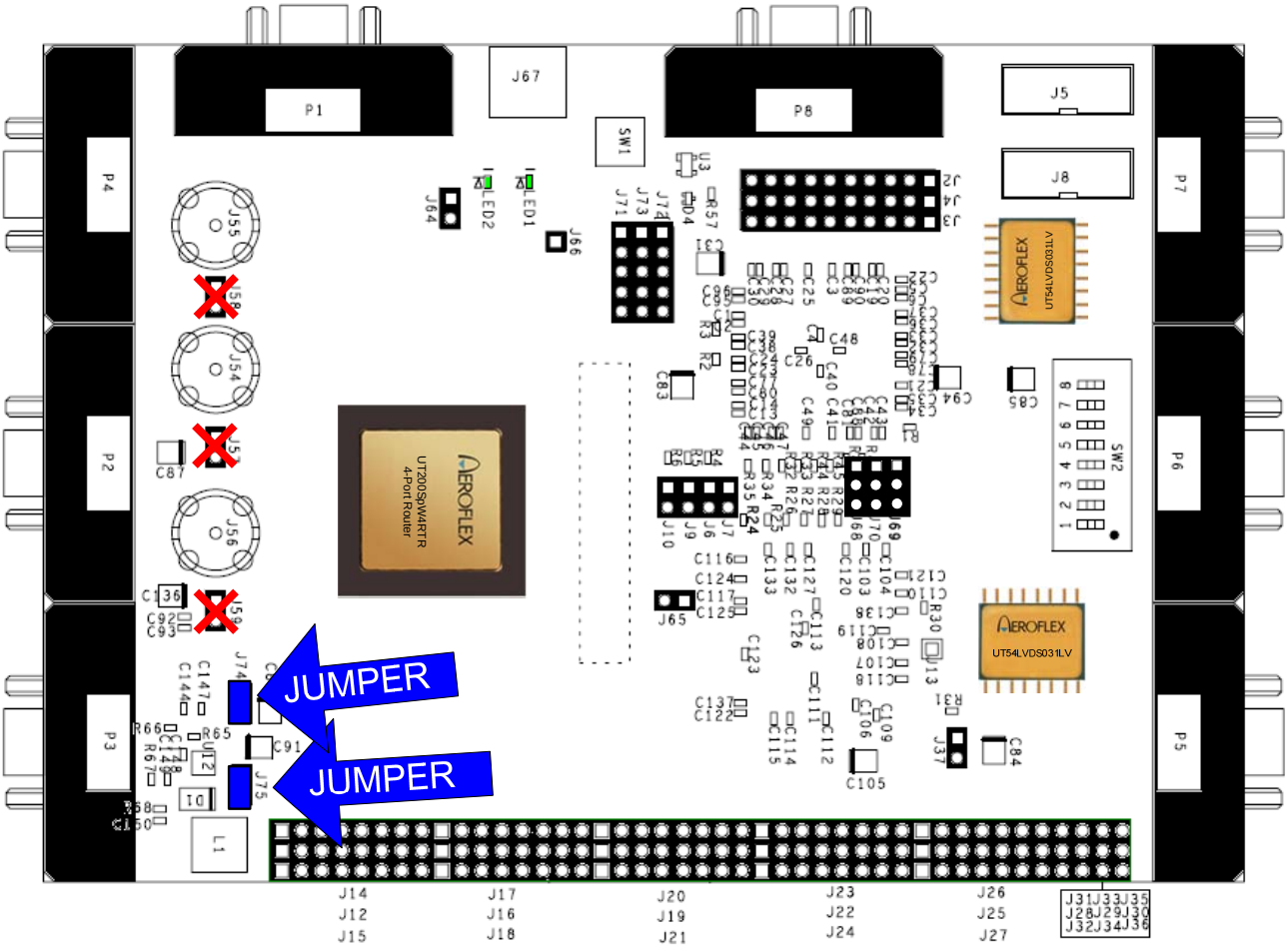

Figure 3. Aeroflex Gaisler LEON-3FT Power Jumper Settings

5.2 UT200SpW4RTR 4-Port Router

The 4-Port router can be easily configured using any of the four SpaceWire ports or the Host port connected to the V2. If the user is going to use the XC18V04VQ44 Xilinx PROM (44-VTQFP) with the Virtex 2 - XC2V500 (FG256/FGG256) jumpers should be added to J6, J9, and J10 for proper access from the PROM to the FPGA. Jumpers J6, J9 and J10 are located in the center on the top of the board.

5.2.1 LV_/CM Control Signal

The LV_/CM pin is the enable signal used to select between the LVDS or LVCMOS interfaces on the router. When LV_CM is high the LVDS interface is active. When LV_CM is low, the LVCMOS interface is active.

5.2.1.1 Manual Jumper Control (J70 pin 2)

Control of this pin can be accomplished using the corresponding pin on J70 or through the V2 FPGA. For example, if LV_/CM signal is tied high, the LVDS I/O is active (TX1_D_LV[1:0], TX1_S_LV[1:0], RX1_D_LV[1:0], and RX1_S_LV[1:0]), while the CMOS SpW I/O TX1_D, TX1_S, RX1_D, and RX1_S is tri-stated. The row of pins closest to the LVCMOS SpaceWire connectors is connected to VDD, the row closest to the middle of the board is connected to VSS.

5.2.1.2 V2 Control

The LV_/CM pin can also be controlled using the on board Virtex-2 device. LV_/CM on the UT200SpW4RTR device is connected to pin B7 (IO_L94N_0/VREF_0) on the XC2V500 in the Fine-Pitch BGA (FG256/FGG256) package. Control of the SpW I/O selection pin can be achieved by writing code for the V2 device.

5.2.2 /OE Control Signal

This signal, used to control the outputs of the Receive FIFO, /OE , is active low. /OE supports the memory interface timing of host controller that incorporates multiplexed address and data on the bus. If the user is not going to use the parallel HOST interface, /OE can be held high.

5.2.2.1 Manual Jumper Control (J70 pin 3)

Control of this pin can be accomplished using the corresponding pin on J70 or through the V2 FPGA. Jumpering pin 3 on J70 to VDD disables the HOST port, tying pin 3 on J70 to VSS activates the HOST port. The row of pins closest to the LVCMOS SpaceWire connectors is connected to VDD; the row closest to the middle of the board is connected to VSS.

5.2.2.2 V2 Control

The /OE pin can also be controlled using the on board Virtex-2 device. /OE on the UT200SpW4RTR device is connected to pin D7 (IO_L93N_0) on the XC2V500 in the Fine-Pitch BGA (FG256/FGG256) package. Control of the SpW HOST interface can be achieved by writing code for the V2 device.

5.2.3 /CSEL Control Signal

This allows the state of the control signals for the parallel HOST FIFOs to be connected to internal router logic. If /CSEL is "High", the signals /TX_PUSH, /RX_POP, and any other backend inputs should not be allowed to be passed on to internal logic. If the user is not going to use the parallel HOST interface, /CSEL should be help high.

5.2.3.1 Manual Jumper Control (J70 pin 1)

Control of this pin can be accomplished using the corresponding pin on J70 or through the V2 FPGA. Jumpering pin 1 on J70 to VDD disables the HOST FIFO interface. Tying pin 1 on J70 to VSS activates the HOST port FIFOs. The row of pins closest to the LVCMOS SpaceWire connectors is connected to VDD; the row closest to the middle of the board is connected to VSS.

5.2.3.2 V2 Control

The /CSEL pin can also be controlled using the on board Virtex-2 device. /CSEL on the UT200SpW4RTR device is connected to pin A7 (IO_L94P_0) on the XC2V500 in the Fine-Pitch BGA (FG256/FGG256) package. Control of the SpW HOST interface can be achieved by writing code for the V2 device.

5.2.4 /RST Control Signal

The /RST pin is connected to push button switch SW1. /RST is active low. If the router needs to be reset the user can push this switch and the router resets. After the router is reset the user should ensure that all the configuration and status register are properly set to the desired configuration.

5.2.4.1 Manual Reset Control (SW1)

Control of this pin can be accomplished using switch SW1. pushing SW1 will reset the router device. After the user pushes SW1 they should ensure that all the configuration and status register are properly set to the desired configuration.

5.2.4.2 V2 Control

The /RST pin can also be controlled using the on board Virtex-2 device. /RST on the UT200SpW4RTR device is connected to pin C7 (IO_L93P_0) on the XC2V500 in the Fine-Pitch BGA (FG256/FGG256) package. Control of the SpW HOST interface can be achieved by writing code for the V2 device. After the router is reset the user should ensure that all the configuration and status register are properly set to the desired configuration.

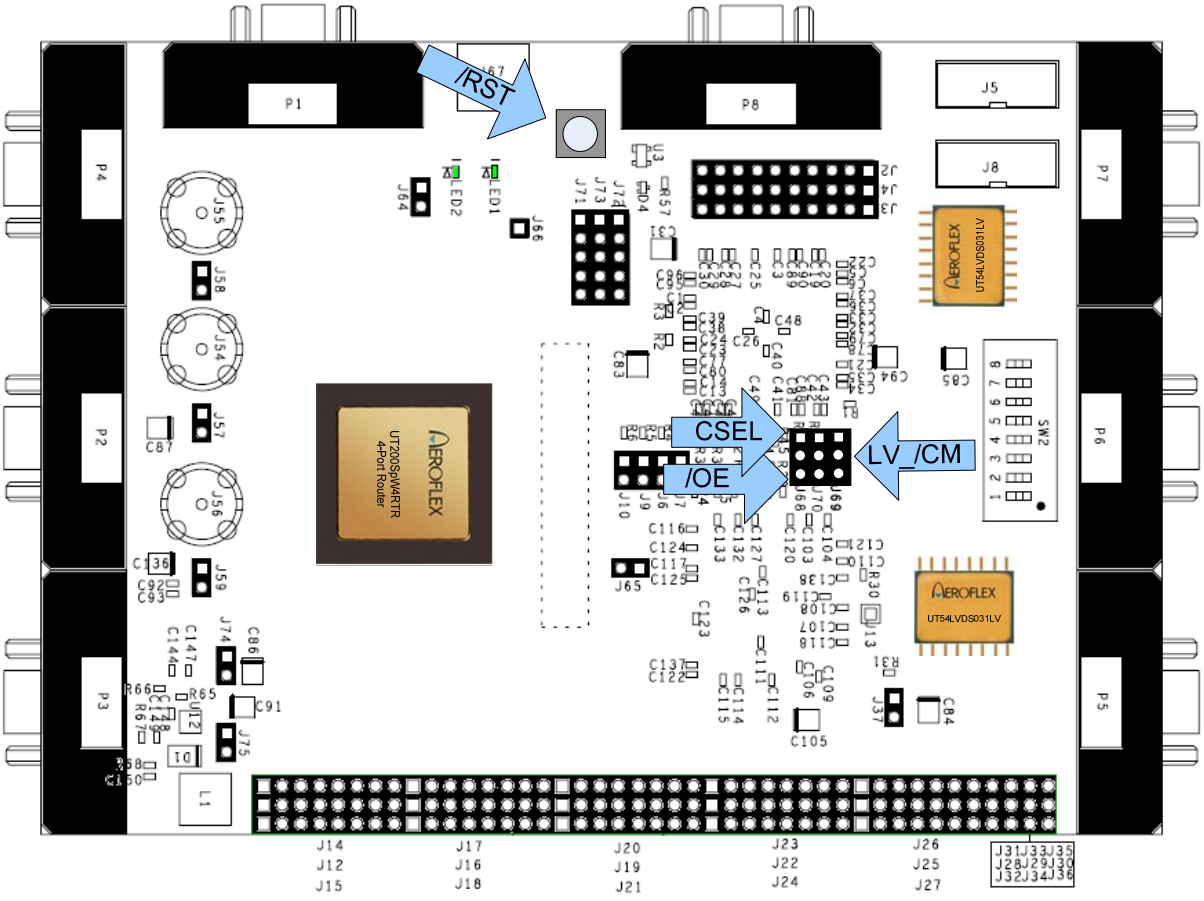

Figure 4. UT200SpW4RTR Control Signal Locations

5.2.5 HOST Port Interface

Access to the 5th port of the HOST port of the UT200SpW4RTR can be accomplished by writing code targeted to the Virtex 2 FPGA. Signals used to access the HOST port are listed below. Access to the HOST port can only be achieved by using the V2. Be sure to jumper headers J6, J9, and J10 to ensure proper access from the PROM to the V2 FPGA.

Table 1. UT200SpW4RTR Transmit HOST Port Connection Table

Virtex 2 – XC2V500 (FG256/FGG256)		UT200WSpW4RTR – 255 LGA	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L01P_0	B4	TXPORT0	C1
IO_L01N_0	C4	TXPORT1	D1
IO_L02P_0	C5	TXPORT2	F1
IO_L02N_0	D5	TXPORT3	G1
IO_L03P_0/VRN_0	A5	TXPORT4	C2
IO_L03N_0/VRP_0	B5	TXPORT5	D2
IO_L04P_0	C6	TXPORT6	E2
IO_L04N_0/VREF_0	D6	TXPORT7	F2
IO_L05P_0	A6	TXPORT8	G2
IO_L05N_0	B6	TX_PUSH	D3
IO_L92P_0	E7	TX_FULL	E3
IO_L92N_0	E6	TX_ALMOST_FULL	F3

Table 2. UT200SpW4RTR Receive HOST Port Connection Table

Virtex 2 – XC2V500 (FG256/FGG256)		UT200WSpW4RTR – 255 LGA	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L01P_1	C13	RXPORT0	A3
IO_L01N_1	B13	RXPORT1	A4
IO_L02P_1	D12	RXPORT2	A6
IO_L02N_1	C12	RXPORT3	A7
IO_L03P_1/VRN_1	B12	RXPORT4	B3
IO_L03N_1/VRP_1	A12	RXPORT5	B4
IO_L04P_1/VREF_1	D11	RXPORT6	B5
IO_L04N_1	C11	RXPORT7	B6
IO_L05P_1	B11	RXPORT8	B7
IO_L05N_1	A11	RX_POP	C4
IO_L92P_1	E11	RXEMPTY	C5
IO_L92N_1	E10	RX_ALMOST_EMPTY	C6

5.2.6 LEON-3FT HOST Port Access

The LEON-3FT evaluation board can also be used to control the FPGA and gain access to the HOST port of the UT200SpW4RTR. The LEON-3FT device can access the UT200SpW4RTR by addressing the pins and signals listed in the following table. This table shows the routing of the signal lines from the LEON-3FT to the Virtex 2 device. The user can write code that will control the Virtex 2 such that the LEON has access to the HOST port of the SpW router.

Table 3. LEON-3FT Evaluation Board Connector (J9) to V2 Connection Table

Virtex 2 - XC2V500 (FG256/FGG256)		LEON-3FT Evaluation Board (J9)	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L05N_5/VRP_5	P6	A0	45
IO_L93P_7/VREF_7	G1	A1	76
IO_L93N_7	G2	A2	44
IO_L94P_7	H3	A3	77
IO_L94N_7	H4	A4	43
IO_L96P_7	H1	A5	78
IO_L96N_7	H2	A6	42
IO_L94N_3	J14	A7	79
IO_L05P_5/VRN_5	N6	A8	39
IO_L94P_3	J13	A9	82
IO_L04N_5	T5	A10	38
IO_L43N_3	L16	A11	83
IO_L04P_5/VREF_5	R5	A12	37
IO_L45P_3	L12	A13	84
IO_L03N_5/D4/ALT_VRP_5	P5	A14	36
IO_L45N_3/VREF_3	K12	A15	85
IO_L03P_5/D5/ALT_VRN_5	N5	A16	35
IO_L06P_3	K13	A17	86
IO_L02N_5/D6	R4	A18	34
IO_L06N_3	L13	A19	87
IO_L02P_5/D7	P4	A20	33
IO_L01P_5/CS	T3	A21	88
IO_L01N_5/RD/WR	T4	A22	32
IO_L43P_3	L15	A23	89
IO_L91P_5/VREF_5	R6	A24	29
IO_L04P_3	M15	A25	92
IO_L91N_5	T6	A26	28
IO_L04N_3	M16	A27	93
IO_L01P_7	D1	D16	94
IO_L01N_7	C1	D17	96
IO_L02P_7/VRN_7	D2	D18	98
IO_L02N_7/VRP_7	D3	D19	102
IO_L03P_7/VREF_7	E3	D20	104
IO_L03N_7	E4	D21	106
IO_L04P_7	E1	D22	108
IO_L04N_7	E2	D23	112
IO_L06P_7	F3	D24	95
IO_L06N_7	F4	D25	97
IO_L43P_7	F1	D26	99
IO_L43N_7	F2	D27	103
IO_L45P_7/VREF_7	G5	D28	105
IO_L45N_7	F5	D29	107
IO_L91P_7	G3	D30	109
IO_L91N_7	G4	D31	113
IO_L0N_3/VREF_3	M14	RESETN (LEON-3FT)	59
IO_L91P_3	K13	BRDYN (LEON-3FT)	58
IO_L03P_3	M13	IOSN (LEON-3FT)	74
IO_L93P_3	K15	READ (LEON-3FT)	75

IO_L91N_3	K14	OEN (LEON-3FT)	47
IO_L93N_3/VREF_3	K16	WRITEN (LEON-3FT)	46
IO_L93P_5	N7	RAMOEN0	66
IO_L93N_5	P7	RAMOEN1	67
IO_L92P_5	M6	RAMSN0	55
IO_L92N_5	M7	RAMSN1	54

5.2.7 SpaceWire Interfaces

5.2.7.1 LVDS Interface

The LVDS SpaceWire ports on the UT200SpW4RTR are connected to SpaceWire connectors located closest to the Router device.

Table 4. LVDS SpaceWire to UT200SpW4RTR port connection table

SpaceWire Port (LVDS)	Connector
1	P1
2	P4
3	P2
4	P3

Termination resistors are present on the receive signals of the LVDS SpW ports. The user is cautioned to be sure to add 100Ω terminations resistors close to the router device when designing a board. Termination resistors are not external and must be external to allow for proper operation of the UT200SpW4RTR device.

5.2.7.2 LVCMOS Interface

The LVCMOS SpaceWire ports on the UT200SpW4RTR are connected to UT54LVDS031LV LVDS Drivers. The UT54LVDS032LV LVDS receivers then run to the SpaceWire connectors located furthest to the Router device. To enable the external LVDS Drivers and Receivers, the user must use SW2 to enable or disable the UT54LVDS031LV and UT54LVDS032LV devices.

Table 5. LVCMOS SpaceWire to UT200SpW4RTR port connection table

SpaceWire Port (LVCMOS)	Connector
1	P5
2	P6
3	P7
4	P8

Table 6. LVDS Driver UT54LVDS031LV Enable configuration

Enable Signal		Input	Output	
EN	**/EN**	**DIN**	**DOUT+**	**DOUT-**
L	H	X	Z	Z
All other combinations of ENABLE signals		L	L	H
		H	H	L

Table 7. LVDS Receiver UT54LVDS032LV Enable Configuration

Enable Signal		Input	Output
EN	**/EN**	**RIN+ - RIN-**	**ROUT**
L	H	X	Z
All other combinations of ENABLE signals		VID≥0.1V	H
		VID≥-0.1V	L
		Fail Safe Mode	H

Table 8. Switch 2 LVDS Devices Connection Table

Switch 2 (SW2)		
Position	**Name**	**Port Enabled**
1	TX 1 ENABLE (EN)	1 and 2
2	TX 1 ENABLEB (/EN)	1 and 2
3	RX 1 ENABLE (EN)	1 and 2
4	RX1 ENABLEB (/EN)	1 and 2
5	TX 2 ENABLE (EN)	3 and 4
6	TX 2 ENABLEB (/EN)	3 and 4
7	RX 2 ENABLE (EN)	3 and 4
8	RX 2 ENABLEB (/EN)	3 and 4

5.2.8 Time Code Interface

The UT200SpW4RTR time code interface is tied to the V2 FPGA. Time code signals can be monitored by writing a user program that looks at these signals.

Table 9. Time code interface connection table

Virtex 2 - XC2V500 (FG256/FGG256)		**UT200WSpW4RTR - 255 LGA**	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L01N_2	C16	TIMECODE1	T3
IO_L01P_2	D16	TIMECODE0	T2
IO_L02N_2/VRP_2	D14	TIMECODE3	R2
IO_L02P_2/VRN_2	D15	TIMECODE2	T4
IO_L03N_2	E13	TIMECODE5	R4
IO_L03P_2/VREF_2	E14	TIMECODE4	R3
IO_L04N_2	E15	TIMECODE7	R6
IO_L04P_2	E16	TIMECODE6	R5
IO_L06N_2	F13	TICKOUT	T7
IO_L06P_2	F14	TICKIN	T6

5.2.9 Clock Interface

The Clock Network Manager (CNM) is used to provide the five clocks to the UT200SpW4RTR device. The clock signals are HOST_CLK, TXCLK_IN_1, TXCLK_IN_2, TXCLK_IN_3, TXCLK_IN_4, and a clock to the V2 FPGA. Please refer to the UT7R2XLR816 Clock Network Manager datasheet for further information.

The 43 pin headers on the board can be used for the configuration of the CNM. Each of the configuration signals are 3-level inputs. The middle row of headers is connected directly to the corresponding signal on the CNM device. The surrounding rows of pins are connected to VDD = 3.3V and VSS = 0.0V.

The UT7R2XLR816 Clock Network Manager Software GUI should be downloaded from www.aeroflex.com/clocks to assist in the proper configuration selection of the clocks that are provided to the SpaceWire router.

5.2.9.1 Manual Jumper Control (43 Pin header)

Control of the CNM can be accomplished using the corresponding pin on the 43 pin connector to set the proper configuration as reported by the UT7R2XLR816 Clock Network Manager Software GUI. The row of pins on the left or on the inside of the board are connected to 3.3V. The pins towards the outside of the board are connected to VSS and the center row is connected to the pin of the CNM. The silkscreen on the board indicates which signal is routed to which pin.

Table 10. UT7R2XLR816 CNM to 43 Pin Header Connection Table

UT7R2XLR816 - 168 LGA		**43 Pin Header**
Signal Name	**Pin**	**Pin**
/CM_LV	H10	1
FREQ_SEL	K11	2
TEST	B2	3
/OE	D9	4
REF_SEL	F3	5
/RST_DIV	F2	6
FB_PS0	J4	7
FB_PS1	K3	8
FB_PS2	K4	9
FB_DS0	L2	10
FB_DS2	J2	11
FB_DS1	K2	12
FB_DS3	H3	13
0Q_DS3	M6	14
0Q_DS2	M5	15
0Q_DS1	L5	16
0Q_DS0	M4	17
0Q_PS1	M2	18
0Q_PS0	L3	19
1Q_DS3	K6	20
1Q_DS2	L7	21
1Q_DS1	K8	22
1Q_DS0	L8	23
1Q_PS1	M2	24
1Q_PS0	L3	25
2Q_DS3	K10	26
2Q_DS2	L10	27
2Q_DS1	L11	28
2Q_DS0	M10	29
2Q_PS1	M9	30
2Q_PS0	L9	31
3Q_DS3	H11	32
3Q_DS2	F10	33
3Q_DS1	F11	34
3Q_DS0	G11	35
3Q_PS1	H12	36
3Q_PS0	J11	37
4Q_DS3	E11	38
4Q_DS2	C12	39
4Q_DS1	D11	40
4Q_DS0	F12	41
4Q_PS1	L12	42
4Q_PS0	J10	43

5.2.9.2 V2 Control

The CNN device can also be controlled using the on board Virtex-2 device. Control of the CNM can be achieved by writing code for the V2 device that address the signals listed in the following table.

Table 11. UT7R2XLR816 CMN to V2 connection table

Virtex 2 - XC2V500 (FG256/FGG256)		**UT7R2XLR816 - 168 LGA**	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L96N_1/GCLK3P	A9	4Q_PS0	J10
IO_L05N_4/VRP_4	N11	4Q_PS1	L12
IO_L95P_0/GCLK6S	C8	4Q_DS0	F12
IO_L95N_0/GCLK7P	D8	4Q_DS1	D11
IO_L96P_0/GCLK4S	A8	4Q_DS2	C12
IO_L96N_0/GCLK5P	B8	4Q_DS3	E11
IO_L94P_4	T10	3Q_PS0	J11
IO_L94N_4/VREF_4	R10	3Q_PS1	H12
IO_L95P_4/GCLK2P	P9	3Q_DS0	G11
IO_L95N_4/GCLK3S	N9	3Q_DS1	F11
IO_L96P_4/GCLK0P	T9	3Q_DS2	F10
IO_L96N_4/GCLK1S	R9	3Q_DS3	H11
IO_L96P_1/GCLK2S	B9	2Q_PS0	L9
IO_L95N_1/GCLK1P	C9	2Q_PS1	M9
IO_L94N_1	A10	2Q_DS0	M10
IO_L94P_1/VREF_1	B10	2Q_DS1	L11
IO_L93N_1	C10	2Q_DS2	L10
IO_L93P_1	D10	2Q_DS3	K10
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IO_L96N_2	H15	1Q_PS1	M2
IO_L45N_2	F12	1Q_DS0	L8
IO_L45P_2/VREF_2	G12	1Q_DS1	K8
IO_L43N_2	F15	1Q_DS2	L7
IO_L43P_2	F16	1Q_DS3	K6
IO_L91P_4	T11	0Q_PS0	L3
IO_L91N_4/VREF_4	R11	0Q_PS1	M2
IO_L92P_4	M10	0Q_DS0	M4
IO_L92N_4	M11	0Q_DS1	L5
IO_L93P_4	P10	0Q_DS2	M5
IO_L93N_4	N10	0Q_DS3	M6
IO_L01N_4/BUSY/DOUT(1)	T14	FB_PS0	J4
IO_L02P_4/D1	R13	FB_PS1	K3
IO_L03P_4/D3/ALT_VRN_4	P12	FB_PS2	K4
IO_L03N_4/D2/ALT_VRP_4	N12	FB_DS0	L2
IO_L04N_4/VREF_4	R12	FB_DS2	J2
IO_L04P_4	T12	FB_DS1	K2
IO_L05P_4/VRN_4	P11	FB_DS3	H3
IO_L91N_2	G13	FREQ_SEL	K11
IO_L91P_2	G14	/CM_LV	H10
IO_L93N_2	G15	/OE	D9
IO_L93P_2/VREF_2	G16	TEST	B2
IO_L94N_2	H13	REF_SEL	F3
IO_L94P_2	H14	/RST_DIV	F2

5.2.9.3 Initialization Divide Registers

All SpaceWire ports follow the initialization procedure as defined in ECSS-E-ST-50-12C. Following are the key components of the initialization process. After a reset or disconnect the link initiates operation at a signaling rate of 10 Mbps, ±1 Mbps. This provides the system with a common data rate while the system is checked for proper operation. Once the operation of the system is validated each of the four ports switches to the specified transmit data rate. Each of the four ports must be capable of running at 10 ± 1 Mbps.

The initialization divide registers will all be loaded with the jumper settings value that pins TX_DIV[4:0] on the UT200SpW4RTR are set to. These pins must be set to the proper settings in order for the router to initialize at 10Mbps ± 1Mbps as defined in the SpaceWire Standard. The user can use connector 73 or choose to use the V2 FPGA to configure the initialization divide registers.

If the user wishes to configure the router through port 3 and the transmit speed will be 100Mbps, the user will need to set TX_DIV to 0x0A or 10 in decimal. Port 3 has the correct divider for the 10Mbps clock and can initialize the SpaceWire link. If the other ports are transmitting at different data rates, the 10Mbps initialization data rate will not be correct. The user will then use Port 3 to set the Transmit 10Mbps Register to the initialization data rate of 10Mbps. Once the router had initialized and is in the run state, it will begin running at the specified TXCLK_IN rate.

NOTE: if TX_CLK is set to less than 10Mbps the Initialization Divide Register must be set to 0x01. The 4-Port Router will be able to initialize at these data rates. The user needs to be aware; however, to be careful not to send any data until the links are in the run state. If the initialization data rates are different, one side of the link could reach the run state before the other and, if that link begins to send data, there is a good possibility the other side will disconnect because it received a normal character before reaching the run state.

5.2.9.3.1 Manual Jumper Control (J73 header)

Configuration of the initialization divide registers can be accomplished using the corresponding pin on the 5 pin J73 connector. The row of pins closest to the LVCMOS SpW ports on the UT200SpW4RTR connected to 3.3V. The pins towards the LVDS SpW ports are connected to VSS and the center row is connected to the initialization divide pin as shown in the following table.

Table 12. J73 Initialization Divide Register pin assignments

UT200SpW4RTR – 255 LGA		**J73 Header**
Signal Name	**Pin**	**Pin**
TX_DIV[0]	M2	1
TX_DIV[1]	L2	2
TX_DIV[2]	K2	3
TX_DIV[3]	J3	4
TX_DIV[4]	H3	5

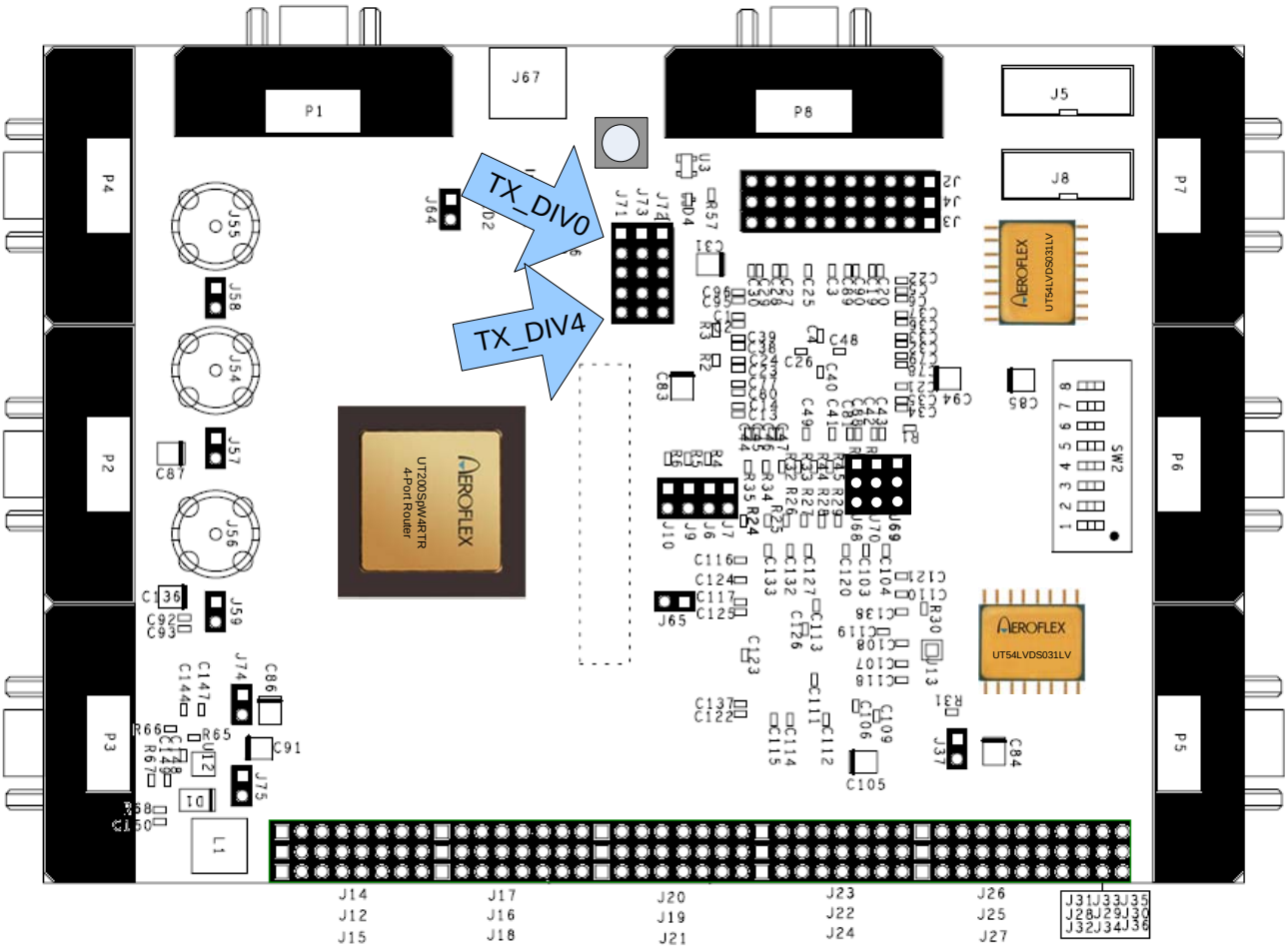


Figure 5. TX_DIV[4:0] Jumper Locations

5.2.9.3.2 V2 Control

The Initialization Divide Registers can also be controlled using the on board Virtex-2 device. Control of the TX_DIV[4:0] pins can be achieved by writing code for the V2 device that address the signals listed in the following table.

Table 13. UT200SpW4RTR TX_DIV[4:0] to V2 Connection Table

Virtex 2 - XC2V500 (FG256/FGG256)		**UT200WSpW4RTR - 255 LGA**	
Signal Description	**Pin**	**Signal Name**	**Pin**
IO_L91P_6	K4	TX_DIV4	H3
IO_L91N_6	K3	TX_DIV3	J3
IO_L93P_6	K2	TX_DIV2	K2
IO_L93N_6/VREF_6	K1	TX_DIV1	L2
IO_L94P_6	J4	TX_DIV0	M2

5.2.9.4 Clock Network Manager Configuration

Each of the Divide Select banks contain output division selector and controller pins. There are four ternary inputs used to control the 0Q[1:0], 1Q[1:0], 2Q[1:0], 3Q[1:0], 5Q[1:0], 7Q[1:0], and FB_DS[1:0] output clock dividers, inverters, and enable controls. See Table 1 in the UT7R2XLR816 Clock Network Manager Datasheet for output behavior resulting from each combination of these pins.

The #Q_PS# pins are the bank output phase selectors. Depending on required skew these bits will need to be set. These two ternary inputs are used to control the 0Q[1:0], 1Q[1:0], 2Q[1:0], 3Q[1:0], 5Q[1:0], 7Q[1:0], and FB_DS[1:0] output phase alignment. See Table 2 in the UT7R2XLR816 CNM Datasheet for output behavior output phase selections resulting from each combination of these pins.

Table 14. The Signal Highlighted in blue is the Signal Used to Clock TXCLK_IN_1

	PIN#	CNM NAME
TXCLK_IN_1	N4	0Q0
	N3	0Q1
	M6	0Q_DS3
	M5	0Q_DS2
	L5	0Q_DS1
	M4	0Q_DS0
	M2	0Q_PS1
	L3	0Q_PS0

Table 15. The Signal Highlighted in blue is the Signal Used to Clock TXCLK_IN_2

	PIN#	CNM NAME
TXCLK_IN_2	N8	1Q0
	N7	1Q1
	K6	1Q_DS3
	L7	1Q_DS2
	K8	1Q_DS1
	L8	1Q_DS0
	L6	1Q_PS1
	K5	1Q_PS0

Table 16. The Signal Highlighted in blue is the Signal Used to Clock TXCLK_IN_3

	PIN#	CNM NAME
TXCLK_IN_3	N12	2Q0
	N11	2Q1
	K10	2Q_DS3
	L10	2Q_DS2
	L11	2Q_DS1
	M10	2Q_DS0
	M9	2Q_PS1
	L9	2Q_PS0

Table 17. The Signal Highlighted in blue is the Signal Used to Clock TXCLK_IN_4

	PIN#	CNM NAME
TXCLK_IN_4	J13	3Q0
	K13	3Q1
	H11	3Q_DS3
	F10	3Q_DS2
	F11	3Q_DS1
	G11	3Q_DS0
	H12	3Q_PS1
	J11	3Q_PS0

Table 18. The Signal Highlighted in blue is the Signal Used to Clock HOST_CLK and the purple Highlighted Signal is Used to Clock the V2

	PIN#	CNM NAME
HOST_CLK and V2_CLK	D13	4Q0
	E13	4Q1
	E11	4Q_DS3
	C12	4Q_DS2
	D11	4Q_DS1
	F12	4Q_DS0
	L12	4Q_PS1
	J10	4Q_PS0

Table 19. The feedback signals connects to the internal Phase- Frequency Detector

	PIN#	CNM NAME
FEEDBACK	H3	FB_DS3
	J2	FB_DS2
	K2	FB_DS1
	L2	FB_DS0
	K4	FB_PS2
	K3	FB_PS1
	J4	FB_PS0

Tables 14-19 show the CMN banks that must be considered when using the CMN software to configure the desired clocking of the 4-Port router. An example of how to determine the configuration settings of the CMN is provided below.

5.2.9.5 CMN Configuration Example

Assume the user wanted to provide 200MHz clock to the TXCLK_IN_1, 16MHz clock to the HADS3 Board, 16MHz clock to the HADS3 Board, and 12MHz to the HADS4 board. Given that the Clock Network Manager II oscillator runs at 16MHz, the LCB FPGA will run at 16MHz, and the LEON3FT can run at 16 or 32MHz.

Using the UTR2XLR816 Clock Network Manager II Frequency and Skew Calculator a schematic detailing the output bank configuration requirements will be given. The output from the Frequency and Skew Calculator will be used to configure the Clock Network Manager II register at location 0x00002000 to 0x00002018.

UTR2XLR816 Clock Network Manager II Frequency and Skew Calculator use the input the Input Frequency Ref to 50MHz. There is a 50MHz oscillator that is used as the clock input reference.

Click [Configure] button

Bank 0 200
Bank 1 200
Bank 2 100
Bank 3 100
Bank 4 50 (HOST_CLK must be set to 0.25 times the fastest TXCLK_IN)
Bank 5 Don't Care
Bank 6 Don't Care
Bank 7 Don't Care

Click [Calculate Configuration]
Select the configuration that best meets the systems needs.
Click [Return Selected Configuration]

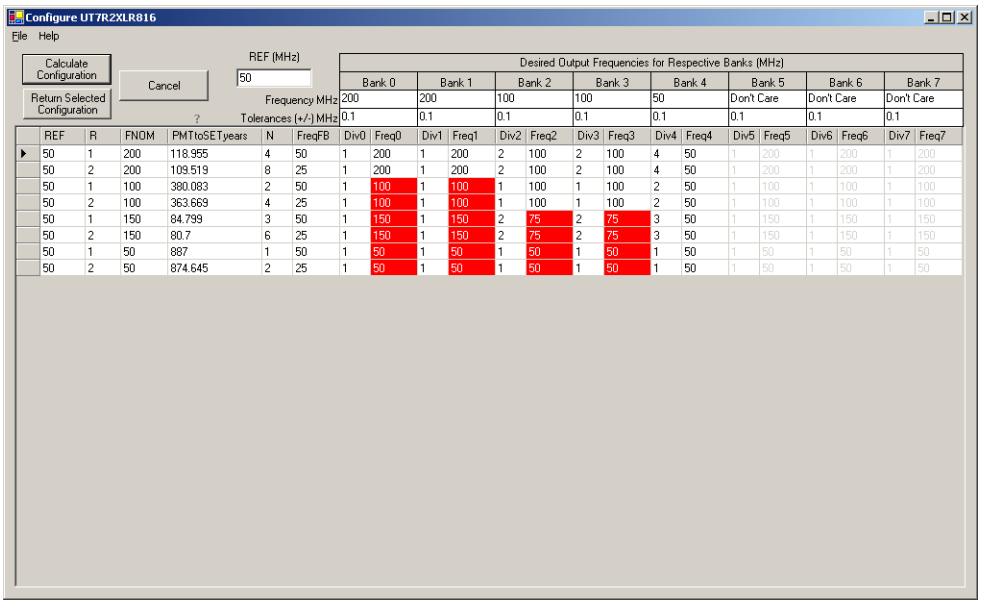


Figure 6. UTR2XLR816 Clock Network Manager II Frequency and Skew Calculator results options

Click [Refresh Configuration]
Click [View Schematic]

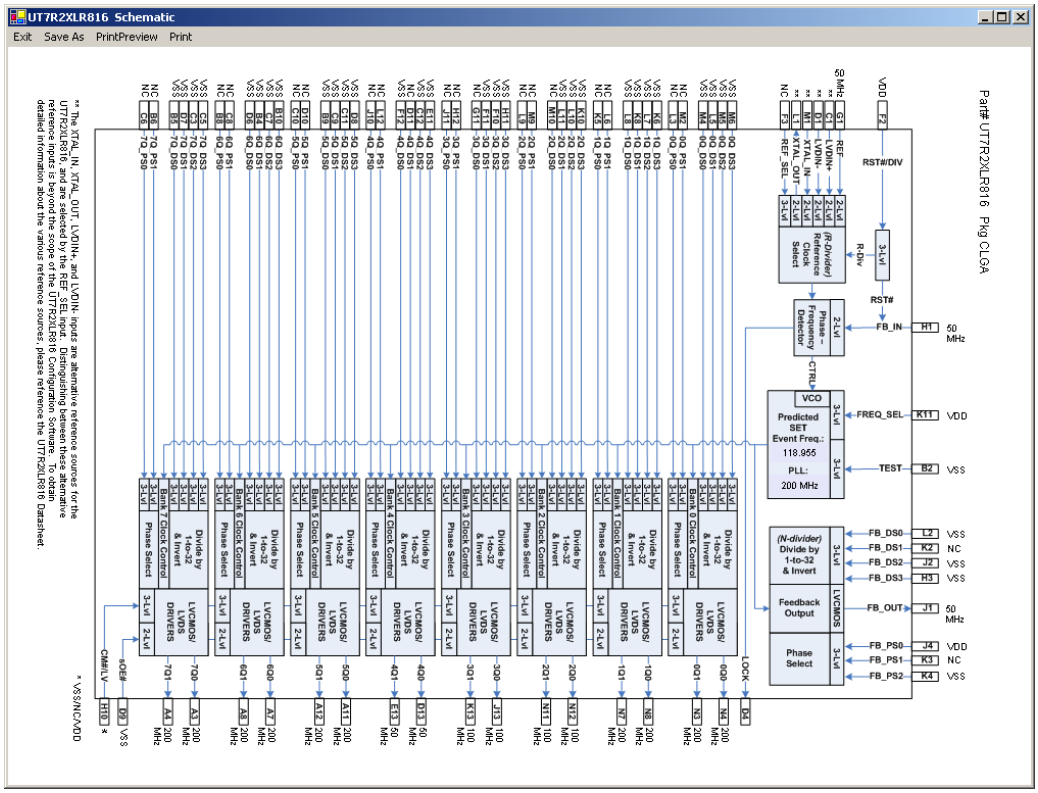


Figure 7. Configuration Schematic

This is the configuration schematic that will be used to configure the Clock Network Manager for the clocking of the UT200SpW4RTR and the V2 FPGA.

Table 20. Details the header pin configuration for the example of how to configure the CMN

VSS = connect the center pin to the VSS pin next to it
VDD = connect the center pin to the DD pin next to it
NC = Do not connect the center pin to anything

Header Pin	CNM Pin	Value
7	FB_DS0	VSS
8	FB_DS1	NC
9	FB_DS2	VSS
10	FB_DS3	VSS
11	FB_PS0	VDD
12	FB_PS1	NC
13	FB_PS2	VSS
14	0Q_DS0	VSS
15	0Q_DS1	VSS
16	0Q_DS2	VSS
17	0Q_DS3	VSS
18	0Q_PS0	NC
19	0Q_PS1	NC
20	1Q_DS0	VSS
21	1Q_DS1	VSS
22	1Q_DS2	VSS
23	1Q_DS3	VSS
24	1Q_PS0	NC
25	1Q_PS1	NC
26	2Q_DS0	NC
27	2Q_DS1	VSS
28	2Q_DS2	VSS
29	2Q_DS3	VSS
30	2Q_PS0	NC
31	2Q_PS1	NC
32	3Q_DS0	NC
33	3Q_DS1	VSS
34	3Q_DS2	VSS
35	3Q_DS3	VSS
36	3Q_PS0	NC
37	3Q_PS1	NC
38	4Q_DS0	VSS
39	4Q_DS1	NC
40	4Q_DS2	VSS
41	4Q_DS3	VSS
42	4Q_PS0	NC
43	4Q_PS1	NC

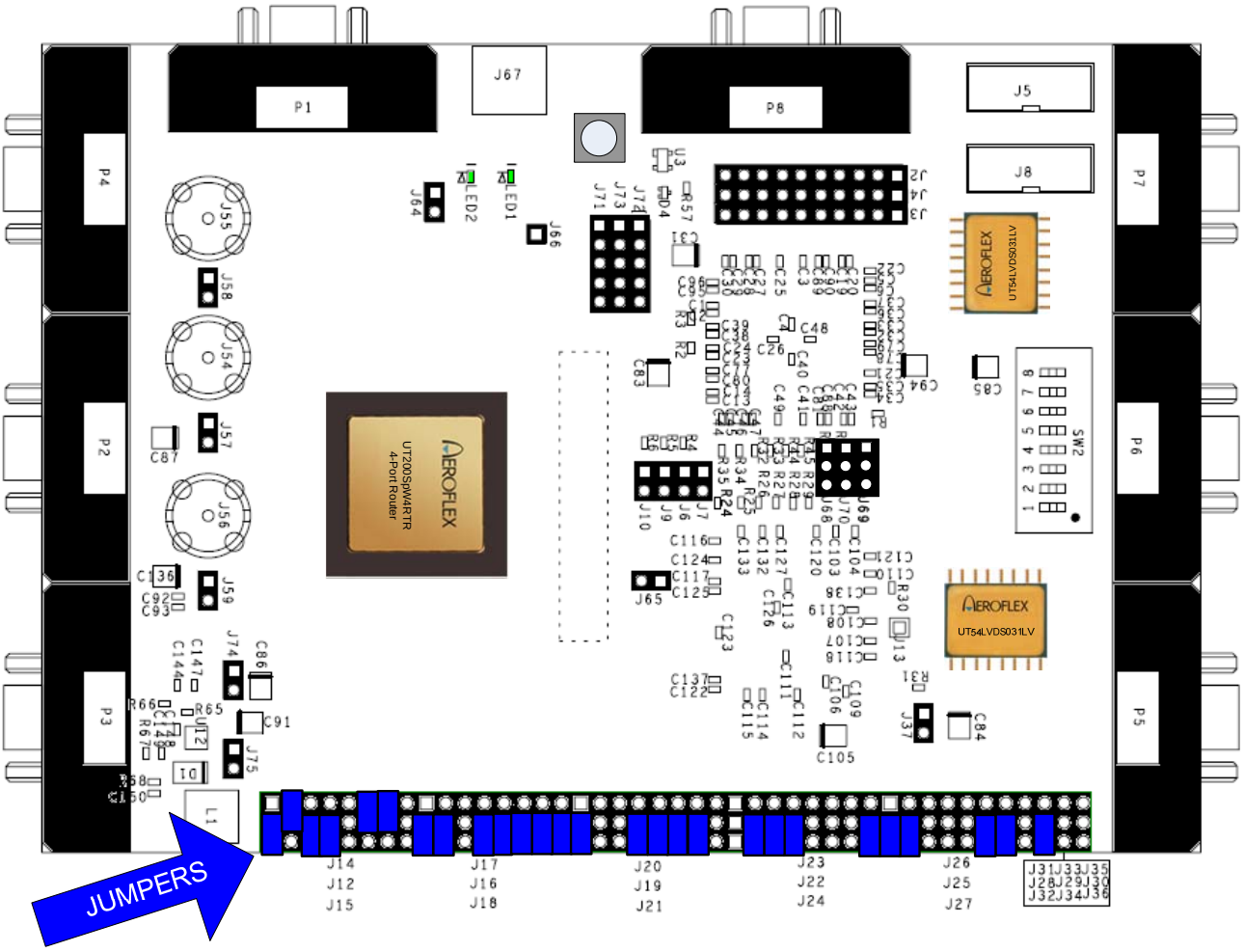


Figure 8. Example CNM Jumper Setting

5.2.9 Router Configuration Protocol

The user may want to access to the configuration and status registers. Access to these registers can be accomplished though any one of the four SpaceWire ports or the External Port. The default configuration is for all ports to be configuration ports. If one or more ports are set up to be configuration ports, only one configuration command should be sent at a time.

5.2.9.6 Configuration Ports

If multiple ports are set up as configuration ports and more than one configuration command is being sent within the router, the configuration packets will be corrupted. The first byte of data with value 0x00 received by any router port after reset or an EOP/EEP initiates a configuration transaction. (ECSS-E-ST-50-12C). Configuration transactions allow access to the lookup tables, configuration registers and status registers. The packet protocols for configuration reads and writes are specified in the following sections.

5.2.9.7 Configuration Write

A configuration write packet loads a 16-bit data word to the specified 16-bit address location in the configuration memory space. A configuration write packet begins with zero (0x00) or can contain additional router address bytes, followed the final destination address byte set to zero. A Configuration Write packet is shown below.

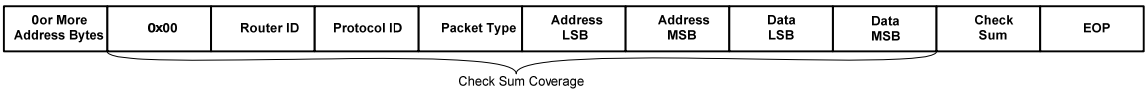


Figure 9. Configuration Write Command

Next, the router ID byte should be set to the value in the receiving router ID register. The Packet Type byte should be set to Write (see table 6.), followed by the address least significant byte, the address most significant byte, then the data least significant byte and the data most significant byte. The last byte before the end of packet (EOP) will be the arithmetic Checksum value, which is an arithmetic sum of the final destination address, the router ID, the Packet Type, the Address and Data bytes. If the checksum value does not match, the command will not be executed. If the packet has less than eight (8) bytes or the Checksum value is not the last byte, the command will not be executed. (ECSS-E-ST-50-12C).

5.2.9.8 Configuration Read

The Read packet will read a number (Count) of 8-bit data values from consecutive 16-bit address locations and transmit the data to the return location specified. This packet begins with zero or more hardware or logical address bytes followed by the final destination address byte set to zero.

Next, the router ID byte should be set to the value in the router ID register, unless the router ID is being read. The Packet Type byte should be set to Read, (0x01 or 0x02) followed by the address least significant byte, the address most significant byte, the word count byte, and one or more return path address byte(s). The order of the return path address bytes are to read in the order they are received.

That is to say, the first return path address byte will be the path out of the first router with subsequent bytes to be used for the next layers of routers. The last byte will be the checksum value, which is an arithmetic sum of the destination address, router ID, packet type, address bytes, data bytes and return path bytes. If the checksum received does not match the calculated value, an error end of packet will be sent to the return address. The word count byte must be greater than zero. A value of zero causes the command to not be executed. The return address path must contain one or more bytes and the first header byte must not be zero; otherwise, the command will be considered invalid and not be executed. The following figure shows the bytes required for a Read Packet Command.

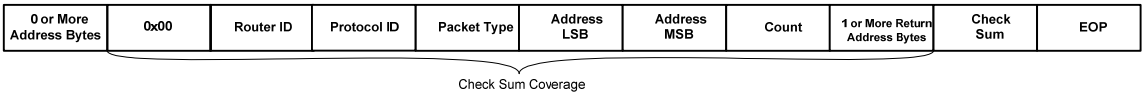


Figure 10. Configuration Read Command

5.2.9.9 Configuration Read Response

A read response will be sent back to the requesting address after a Read command is executed. The Read packet command as shown in Figure 5 sets, up the address to read data from (Address LSB/MSB) and how many 8-bit values to read (Count), and the return address bytes path. After the Read command is executed a Read Response command will be issued and contains the data byte pairs read from the specified address. A read response packet is shown below.

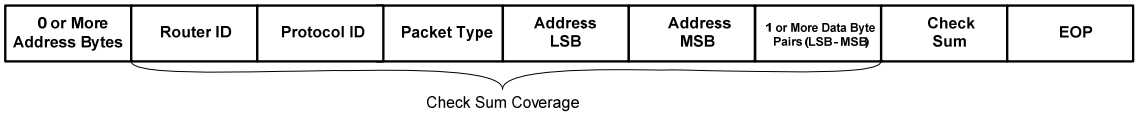


Figure 11. Configuration Read Response Command

NOTE: Please see UT200SpW4RTR Datasheet for more information

5.2.9.10 Router Configuration Example

Assume the user would like to write a value into the Configure Port Enable Register residing at location 0x0102. Assume the user wants to configure the router such that only the HOST port of the router can be used to send configuration packets. Configuring only one configuration port on a router will prevent configuration packets being corrupted when multiple ports are set up as configuration ports. If more than one port is set up as a configuration port and more than one configuration command is sent within the router, the configuration packets will be corrupted. The following example will show how to configure the UT200SpW4RTR Router such that the System or HOST port is enabled and SpaceWire ports 1 to 4 are disabled for configuration of the router.

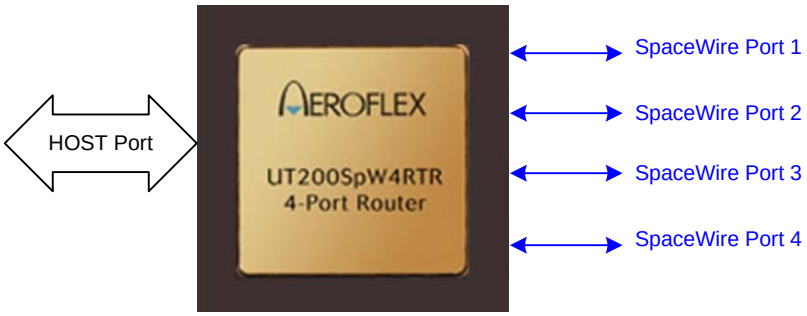


Figure 12. 4-Port Router configuration for the following configuration example

Assume the user wants to write to the Configure Port Enable register in the Router. The user is communication with the router via the HOST port or port 5. The first step is to use the write configuration protocol to write the following packet into port 5 (HOST Port) of the router.

- Use Write configuration protocol into port 5 of the router
- Address Bytes: NONE Needed
- 0x00 for configuration
- Router ID: 00 for router (default)
- Protocol ID: 00 for no protocol used
- Packet Type: 00 is Write
- Set up Data Format
    - Address LSB: 02 LSB
    - Address MSB: 01 MSB of register location 0x0102
- Write in Data
    - Data LSB: 10 Bit15 8 7 4 0
    - Data MSB: 00 00000000 00010000
- Checksum: 13 this is the sum of the final destination address, router ID, protocol ID, packet type, and the address and data bytes. 0x00+0x00+0x00+0x00+0x02+0x01+0x10+0x00 = 0x13
- EOP: 100000000

	00	00	00	00	02	01	10	00	13	100000000
0 or More Address Bytes	0x00	Router ID	Protocol ID	Packet Type	Address LSB	Address MSB	Data LSB	Data MSB	Check Sum	EOP

EOP	1	0	0	0	0	0	0	0	0	
Check Sum	0	0	0	0	1	0	0	1	1	0x13
Data MSB	0	0	0	0	0	0	0	0	1	0x00
Data LSB	0	0	0	0	0	1	0	1	0	0x10
Address MSB	0	0	0	0	0	0	0	0	1	0x01
Address LSB	0	0	0	1	0	0	0	1	0	0x02
Packet Type	0	0	0	0	0	0	0	0	0	0x00
Protocol ID	0	0	0	0	0	0	0	0	0	0x00
Router ID	0	0	0	0	0	0	0	0	0	0x00
0x00	0	0	0	0	0	0	0	0	0	0x00
	8								0	

5.2.10 Configuration and Status Registers

Please see UT200SpW4RTR datasheet available at www.aeroflex.com/Spacewire for detailed information on user configurable registers. The router has a number of configuration and status registers which are used for initial setup of the router and for monitoring the router's performance. These registers can be accessed using the configuration protocol as explained in section 5.2.5.

5.2.11 Other Registers

All the other registers of the UT200SpW4RTR are not required to get the device up and running. The other registers add important status and configuration capabilities, but are not required to start using the router. Please refer to section 6.0 in the UT200SpW4RTR datasheet for a further description of the available registers.

6.0 PORT ADDRESSING

6.1 Path Addressing

Path Addressing is defined as a series of one or more characters at the start of the packet that define the route, or path, that the packet should take across a SpaceWire network. The destination address is specified as a sequence of router output port numbers used to route the packet across the network. The drawback is that the destination address can become relatively large if several routing switches have to be traversed. Path Addressing is used for configuration of the router. The routers look up tables does not have to be configured when path addressing is being used.

A packet with header 0x01 will be routed to Router port 1, a 0x02 header will be routed to port 2, 0x03 will be routed to port 3, and so on. Please see the following table for a list of valid path addresses.

Table 21. Path Address Byte Memory Map

Address Byte (HEX)	Port
0x01	Path Address for Port 1
0x02	Path Address for Port 2
0x03	Path Address for Port 3
0x04	Path Address for Port 4
0x05	Path Address for HOST port

6.2 Logical Addressing

The router can be configured to use Logical addressing by using path addressing to configure the look up tables. Logical Addressing contains a character at the start of a packet, which identifies a look up table location and then selects the destination for the packet. Each destination address has a unique number or logical address associated with it. These numbers can be assigned arbitrarily to nodes provided.

To access logical routing the user must configure the look-up tables. The looks up tables in the 4-Port router have even parity. Valid look up table address locations are 0x0020 to 0x00F. If a portion of the look up table addressing space is not going to be used, it is preferred if the user sets used addressed to 0x00.

6.3 Regional Logical Addressing

This addressing scheme is the same as Logical Addressing except for the fact that header delete is used. When using Regional Logical Addressing the look up tables contains the information on which headers to keep and or delete.

6.4 Group Adaptive

The last SpaceWire addressing scheme is group adaptive. When Group adaptive routing is used, packets can be routed to a requested destination through different network paths. Group adaptive routing can be set up for two paths. To utilize group adaptive routing, the user must configure Group adaptive bits in look-up table. Bits 5 through 9 are group adaptive address, and Bit 11 must be set to 0x01 to enable group adaptive routing. To use Logical or Group Adaptive addressing the router must be configured to set up these functions

6.5 Look Up Table Data Format

The lookup tables on the router are organized into 16-bits and are organized as shown below.

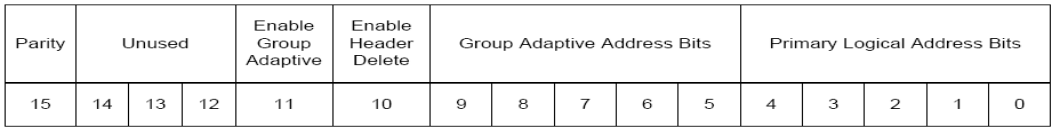


Figure 13. Look-up Table Format

6.5.1 Primary Logical Address Bits

The five LSB bits [4:0] are the Primary Logical Address bits and are for selecting ports 1 through 4 regardless of whether Group Adaptive has been enabled or not. When Group Adaptive has been enabled, the router looks at the port address specified by these bits first and if that port is busy, then looks at the port specified by the Group Adaptive Address Bits.

6.5.2 Group Adaptive Address Bits

Bits [9:5] are used when Group Adaptive has been enabled and the port selected by the Primary Logical Address Bits is busy. If group adaptive routing is not enabled and port selected by the Primary Logical Address Bits is busy, the packet waits until the selected port is free.

6.5.3 Enable Header Delete Bit

Bit [10] is used to enable the header delete function for the port selected by either the Group Adaptive Address bits or the Primary Logical Address Bits. Whenever this bit is set high, the router deletes the header before sending the packet out of the requested transmit port.

6.5.4 Enable Group Adaptive Bit

Bit [11] is used to enable the Group Adaptive function on the router. Setting this bit high tells the router to use bits [9:5] for the port select in the event the port select for the Primary Address Bits is busy.

6.5.5 Unused Bits

Look up table bits [14:12] needs to be set to 0x00. In order for the parity bit to be correct all three unused bits need to contain 0's. If these bits are set to something other than 0x00, the parity calculation will not be the same as what the router is calculating.

6.5.6 Parity Bit

A Parity Bit is included for each lookup table location. The parity is even. When the header byte is decoded and falls between address 0x20 and 0xFF, a lookup table address will be retrieved by the lookup table.

Again, parity will be calculated by adding the number of ones that are contained in the previous 8-bits data. If the total number of 1's in bits added together is odd, the parity is odd parity. And if the number of 1's in bits added is even, the parity is even parity. The current parity bit will then be compared to the calculated parity and if they are not the same, the packet will be read out of the receive FIFO. This is commonly referred to as "Spilling the Packet". Additionally, the Parity Error Register will be incremented.

Parity error register is different from the previously discussed SpaceWire parity. The parity error register is based on the data in the lookup table. Please see ECSS-E-ST-50-12C for more information regarding parity.

6.5.7 Look up table configuration Example 1

Assume the user wants to write to the configure look up table address 0x0020 to contain addressing to send out port 1. Meaning if a packet is received with logical address bytes 0x0020 it will be routed out port 1 of the router. The user is in communication with the router via the HOST port or port 5.

The user will have to use the write configuration protocol into port 5 (HOST Port) of the Primary router to set up look up tables.

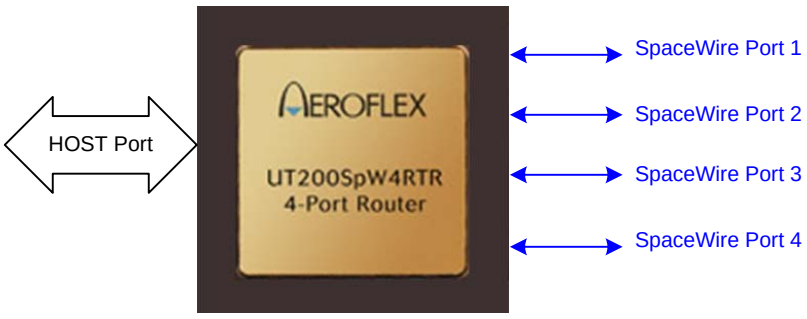


Figure 14. 4-Port Router configuration for the look up table access and configuration example

- Write directly into port 5 of the Router, no Address Bytes required
- 0x00 for configuration
- Router ID: 00 for router ID (default)
- Protocol ID: 00 for no protocol used
- Packet Type: 00 is Write
- Set up look-up table
    - Address LSB: 20 sets up first address in look up table
    - Address MSB: 00 the address MSB is always 00 because the address range of the Logical Addresses is 0x0020 to 0x00FF
- Write in Data
    - Data LSB: 01 sets up port 1 of Router (this will set up logic such that is register 0x0020 is received the data will go out of port 1 on Router)
    - Data MSB: 04 Header Delete set

The write data for the look up table was calculated using the following look up table configuration. Primary Logical Address Bits = 1 for the Logical address to be set to port 1. No group adaptive bits are used. Enable header delete was turned on, and the parity was calculated as 0, because 1+1=2 = even number.

Parity	Unused			Enable Group Adaptive	Enable Header Delete	Group Adaptive Address Bits					Primary Logical Address Bits				
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Data MSB Data LSB

- Checksum: 26 this is the sum of the final destination address, router ID, packet type, and the address and data bytes. 0x00+0x01+0x00+0x20+0x00+0x01+0x04 = 0x26
- EOP: 100000000

	00	01	00	00	20	00	01	04	26	100000000
0 or More Address Bytes	0x00	Router ID	Protocol ID	Packet Type	Address LSB	Address MSB	Data LSB	Data MSB	Check Sum	EOP

The data characters would look like:

	8								0	
EOP	1	0	0	0	0	0	0	0	0	
Check Sum	0	0	0	1	0	0	1	1	0	0x26
Data MSB	0	0	0	0	0	0	1	0	0	0x04
Data LSB	0	0	0	0	0	0	0	0	1	0x01
Address MSB	0	0	0	0	0	0	0	0	0	0x00
Address LSB	0	0	0	1	0	0	0	0	0	0x20
Packet Type	0	0	0	0	0	0	0	0	0	0x00
Protocol ID	0	0	0	0	0	0	0	0	0	0x00
Router ID	0	0	0	0	0	0	0	0	1	0x00
0x00	0	0	0	0	0	0	0	0	0	0x00

6.5.8 Look up table configuration Example 2

Assume the user wants to confirm the configuration write just preformed on look up table address 0x0020 was completed correctly. The user can then use the read configuration command. The following example details hope to accomplish this.

- Address Bytes: 00, receive on port 5 (HOST port)
- 0x00 for configuration command
- Router ID: 00 is router ID (default)
- Protocol ID: 00 for no protocol used
- Packet Type: is Read No Clear 0x01
- Address LSB: 20
- Address MSB: 00 sets up to read from address 0x0020
- Count: 02 will read 2 Bytes of data. Count can only be an even number. To read one register you must enter 0x02, to read 2 registers you must enter 0x04, etc.
- Return Address Bytes: 01 05 out port 1 of Router A, out port 5 Router P
- Checksum: 28 this is the sum of the router ID, packet type, address bytes, count, an return address bytes. 0x00+0x00+0x00+0x01+0x20+0x00+0x02+0x05= 0x28

0	00	00	00	01	20	00	02	05	2	100000000
0 or More Address Bytes	0x00	Router ID	Protocol ID	Packet Type	Address LSB	Address MSB	Count	1 or More Return Address Bytes	Check Sum	EOP

The Data Character would look like:

EOP	1	0	0	0	0	0	0	0	0	
	0	0	0	1	0	1	0	0	0	0x28
	0	0	0	0	0	0	1	0	1	0x05
Count	0	0	0	0	0	0	0	1	0	0x02
	0	0	0	0	0	0	0	0	0	0x00
	0	0	0	1	0	0	0	0	0	0x20
	0	0	0	0	0	0	0	0	1	0x01
	0	0	0	0	0	0	0	0	0	0x00
	0	0	0	0	0	0	0	0	0	0x00
	0	0	0	0	0	0	0	0	0	0x00
	0	0	0	0	0	0	0	0	0	0x00
	8								0	

7.0 FPGA ACCESS

The V2 FPGA can be accessed using the V2 JTAG connection using a JTAG/USB Xilinx pod through the V2 PROM JTAG connector or using the UT699 LEON-3FT on the Aeroflex Gaisler UT699 evaluation board.

Connector J8 is connected to the XC18V04VQ44 Xilinx PROM (44-VTQFP), connector J5 is connected to the JTAG interface on the Virtex 2 - XC2V500 (FG256/FGG256). The user can determine which access route to the V2 is best suited to their needs.

Be sure to jumper headers J6, J9, and J10 to ensure proper access from the PROM to the V2 FPGA.

8.0 QUICK START GUIDE

To quickly get the UT200SpW4RTR-EVB up and running the following steps should be followed

1. Connect headers J57, J59, and J58
    a. This will enable external power supplies to be used
    b. Ensure that headers J64 and J65 are not connected.
2. Connect BNC connectors to J54 3.3V, J56 2.5V , and J55 5.0V
3. Determine which SpW interface you would like to use
    a. LVDS – Connect Pin 2 J70 to VDD
    b. LVCMOS – Connect Pin 2 J70 to VSS
4. Are you going to use the HOST port?
    a. Yes – Set Pin 1 J70 to VSS and Pin 3 J70 to VSS
    b. No – Set Pin 1 J70 to VDD and Pin 3 J70 to VDD
5. Determine the data rate you would like to use to clock the SpaceWire ports
    a. Use the UT7R2XLR816 Clock Network Manager Software GUI to determine the configuration of the signals on the 43 pin connector
    b. Configure the UT7R2XLR816 using the corresponding pin on the 43 pin connector such that you will get the proper TXCLK_IN_#, HOST_CLK, and V2_CLK
    c. Using J73 set the Initialization Divide Register TX_DIV[4:0] such that one of the TXCLK_IN rates initializes the UT200SpW4RTR at 10Mbps ±1Mbps
    d. Hook up your instruments to the SpaceWire ports
    e. Power on the board

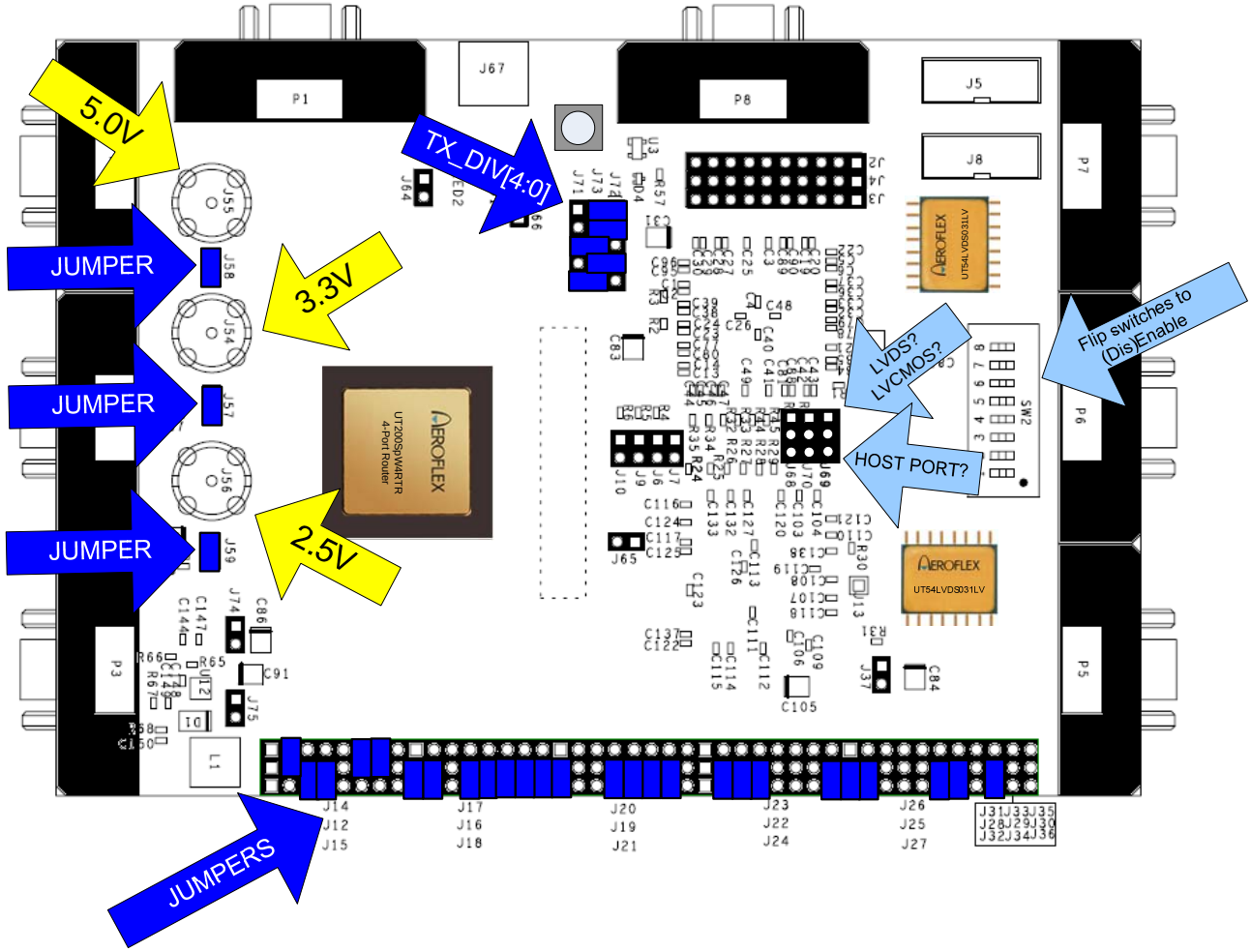


Figure 15. Quick Start example configuration

9.0 COMPATIBILITY WITH GR-UT699 EVALUATION BOARD

The UT200SpW4RTR-EVB can plug directly into the J9 connector on the LEON-3FT evaluation board. A ribbon cable can also be used to easily use the SpaceWire evaluation board with the LEON-3FT board when the LEON board is plugged into a cPCI chassis. Using the ribbon cable to connect the SpaceWire evaluation board to the LEON 3FT GR-UT699 evaluation board allows for easier access to the SpW ports on the UT200SpW4RTR-EVB board.

The virtex-2 FPGA is connected to the HOST port of the UT200SpW4RTR device. J9 on the GR-UT699 evaluation board is also connected to the V2 FPGA; control of the SpW router can be gained by accessing the connections listed in table 3 above.

For further information on interfacing the UT200SpW4RTR-EVB with the GR-UT699 Evaluation board please see the Aeroflex Gaisler GR-UT699 Development Board User Manual.

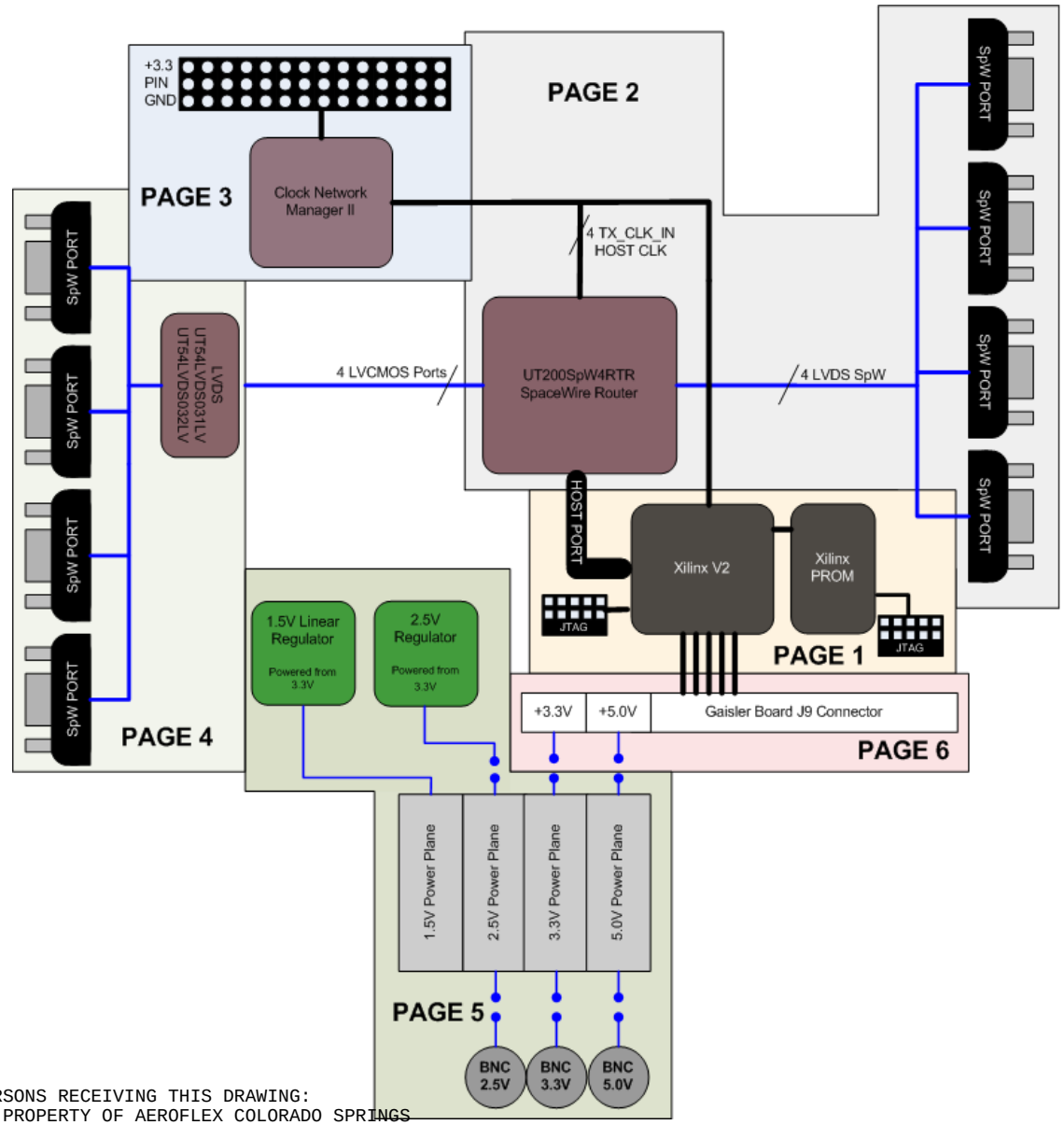
10.0 BOARD SCHEMATICS

The schematics in Appendix A are for reference ONLY.

UT200SpW4RTR-CUSTOMER-EVB Schematic

Change Block

Redesigned board for customer use
Board can plug into Aeroflex/Gaisler LEON-3FT Evaluation Board or be used as a table top board



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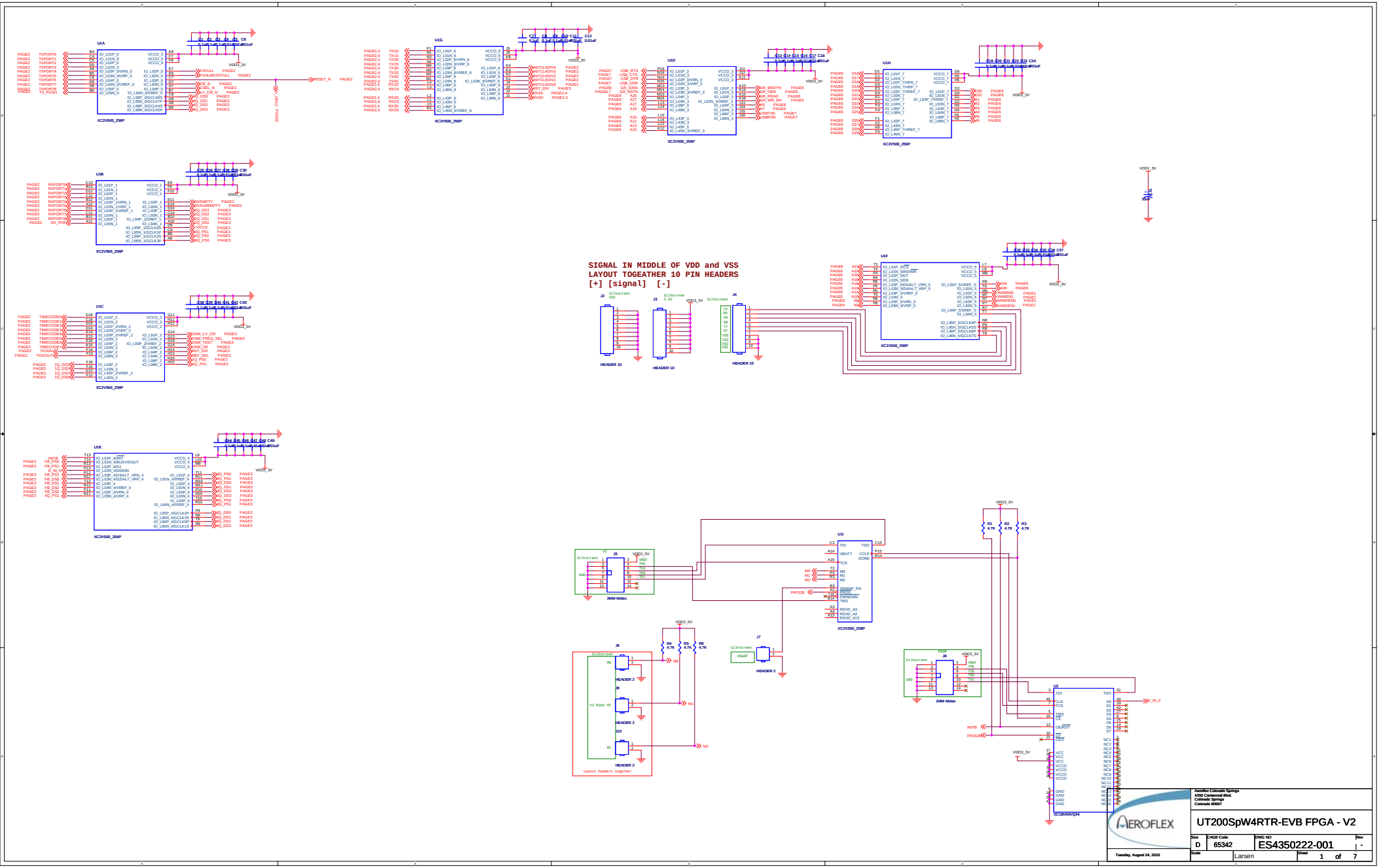
UT200SpW4RTR-CUST_EVB TITLE

Size	CAGE Code	DWG NO	Rev
C	65342	ES4350222-001	-

Tuesday, August 24, 2010 | Scale | Larsen | Sheet 0 of 7


SIGNAL IN MIDDLE OF VDD and VSS
LAYOUT TOGEATHER 10 PIN HEADERS
[+] [signal] [-]
XC2V500_256P
HEADER 10
HEADER 2
2MM Molex
XC18V04VQ44
Layout headers together
UT200SpW4RTR-EVB FPGA - V2
ES4350222-001
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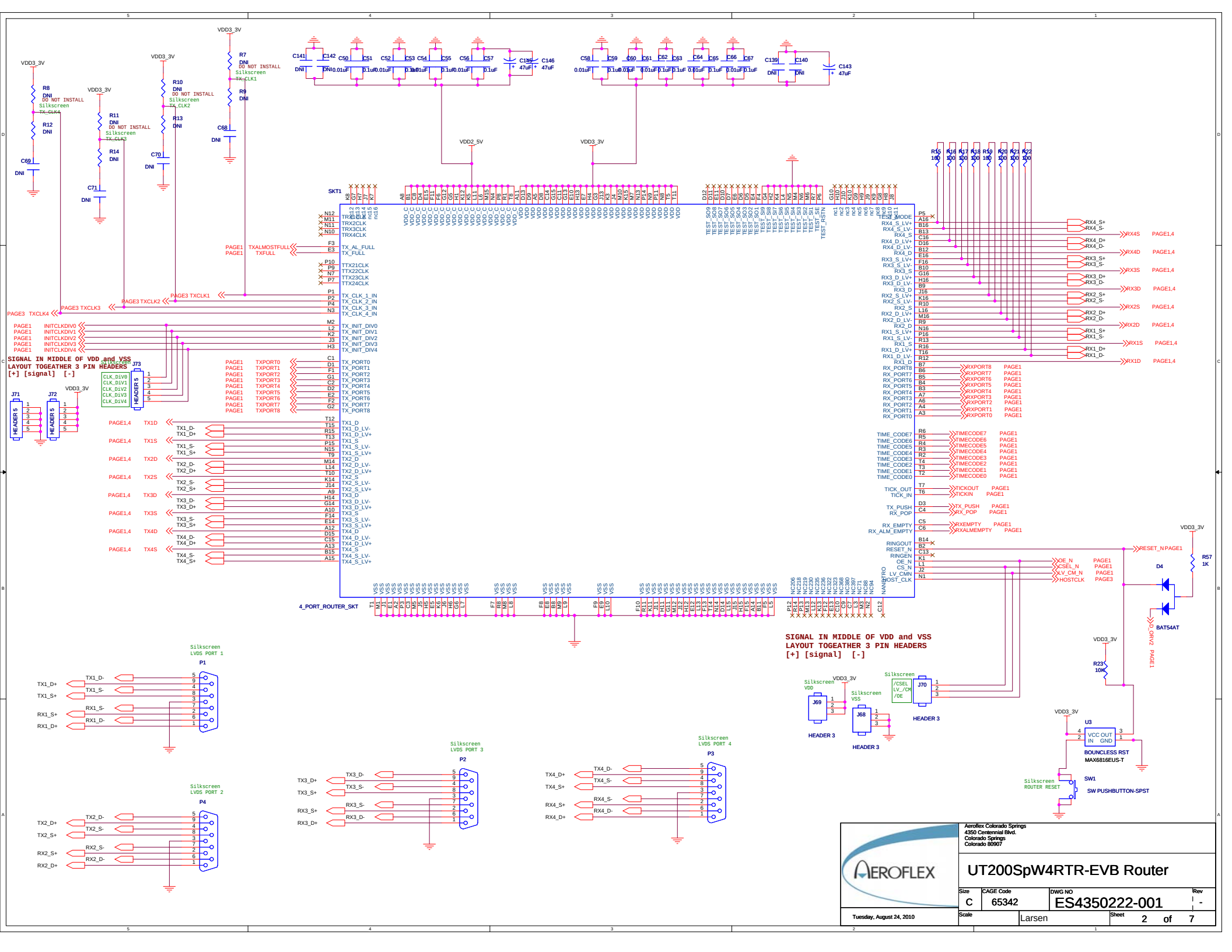
Colorado Springs
Colorado 80907
65342
Tuesday, August 24, 2010
Larsen


SKT1
4_PORT_ROUTER_SKT
SIGNAL IN MIDDLE OF VDD and VSS
LAYOUT TOGEATHER 3 PIN HEADERS
[+] [signal] [-]
SIGNAL IN MIDDLE OF VDD and VSS
LAYOUT TOGEATHER 3 PIN HEADERS
[+] [signal] [-]
Silkscreen LVDS PORT 1
Silkscreen LVDS PORT 2
Silkscreen LVDS PORT 3
Silkscreen LVDS PORT 4
HEADER 3
HEADER 3
HEADER 3
BOUNCLESS RST
MAX6816EUS-T
SW PUSHBUTTON-SPST
BAT54AT
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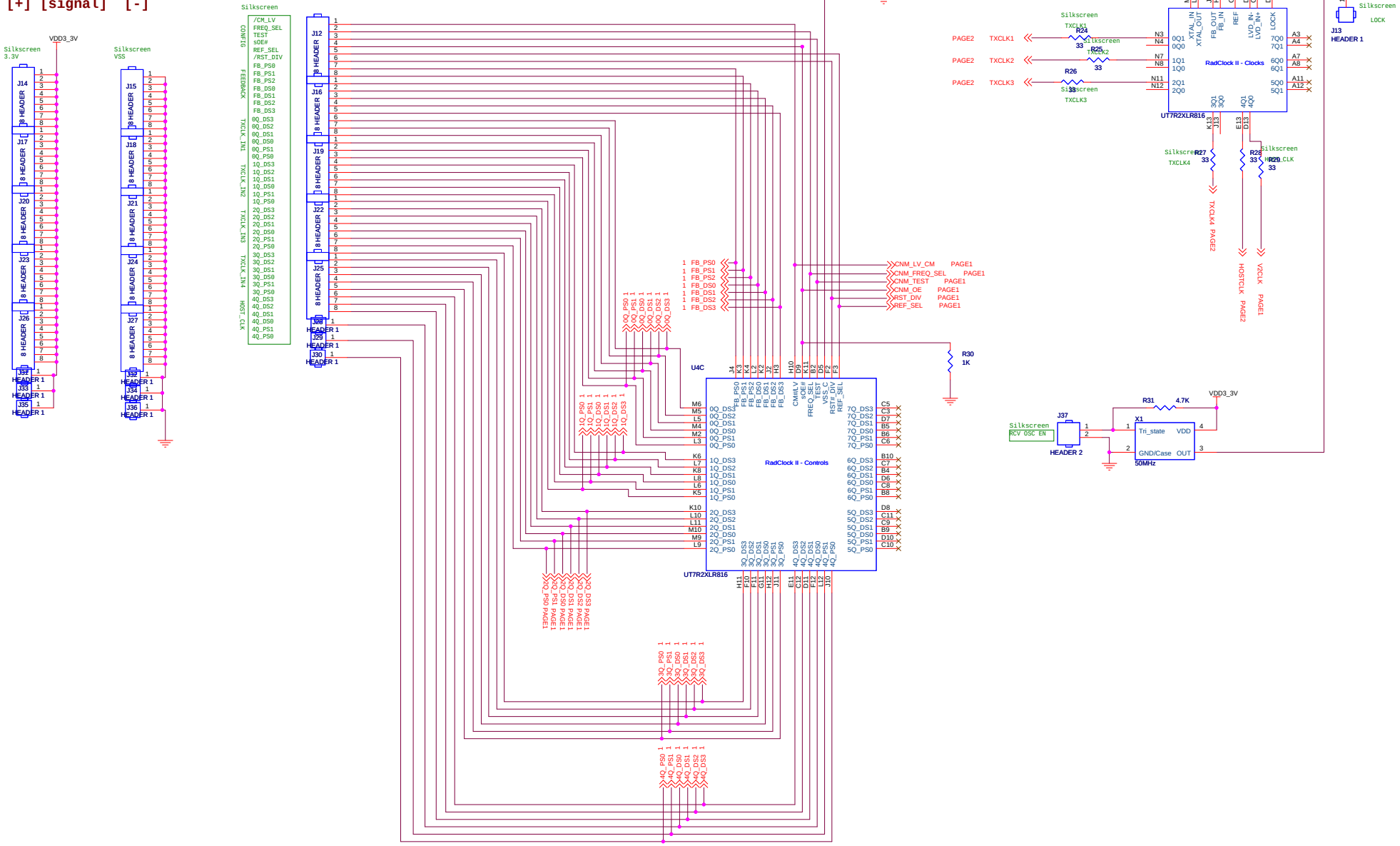
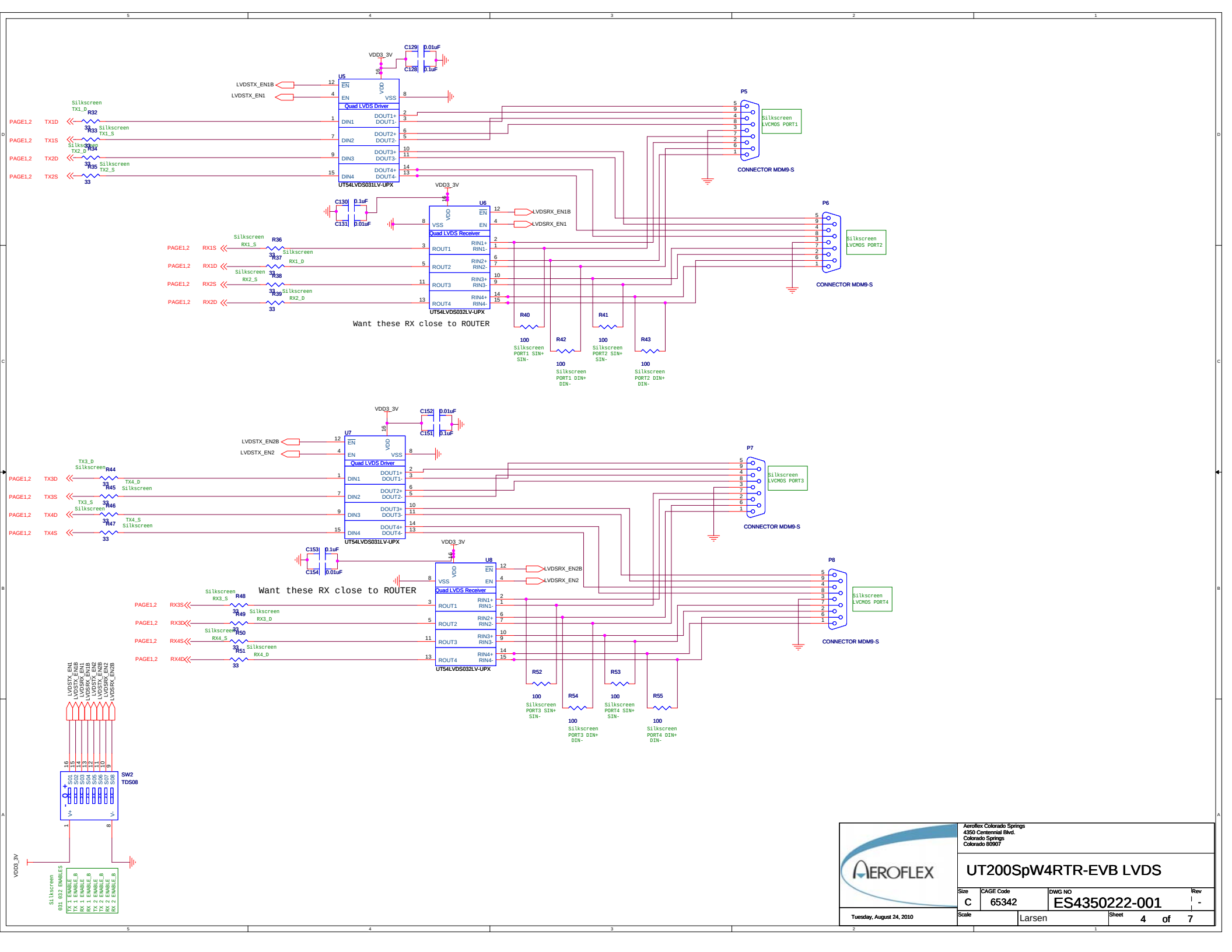
Colorado Springs
Colorado 80907
UT200SpW4RTR-EVB Router
Size C
CAGE Code 65342
DWG NO ES4350222-001
Rev -
Tuesday, August 24, 2010
Scale
Larsen
Sheet 2 of 7

SIGNAL IN MIDDLE OF VDD and VSS
LAYOUT TOGEATHER 43 PIN HEADER
[+] [signal] [-]



Aeroflex Colorado Springs 4350 Centennial Blvd. Colorado Springs Colorado 80907			
UT200SpW4RTR-EVB CLK Management			
Size: C	CAGE Code: 65342	DWG NO: ES4350222-001	Rev: -
Tuesday, August 24, 2010	Scale	Larsen	Sheet: 3 of 7



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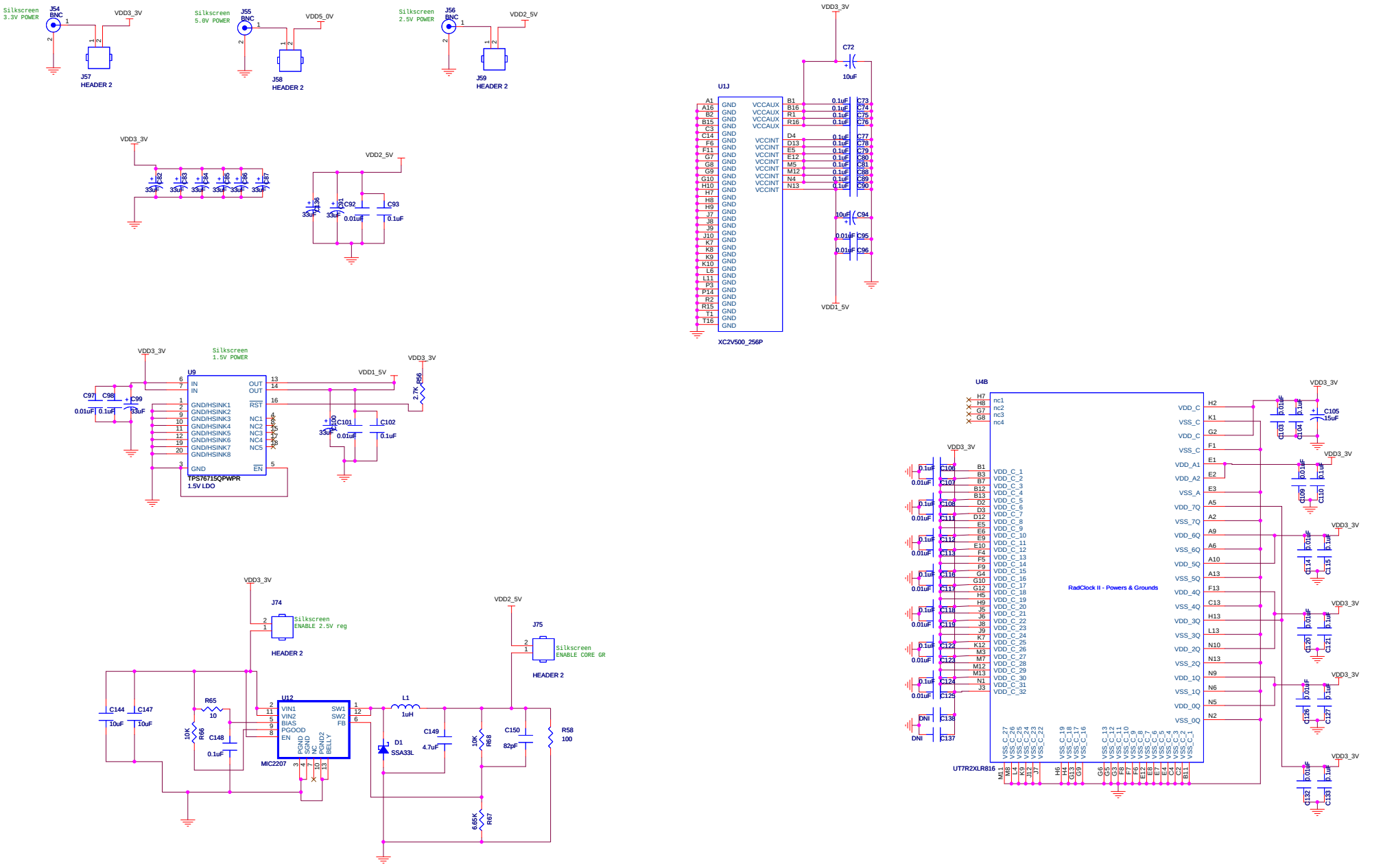
UT200SpW4RTR-EVB LVDS

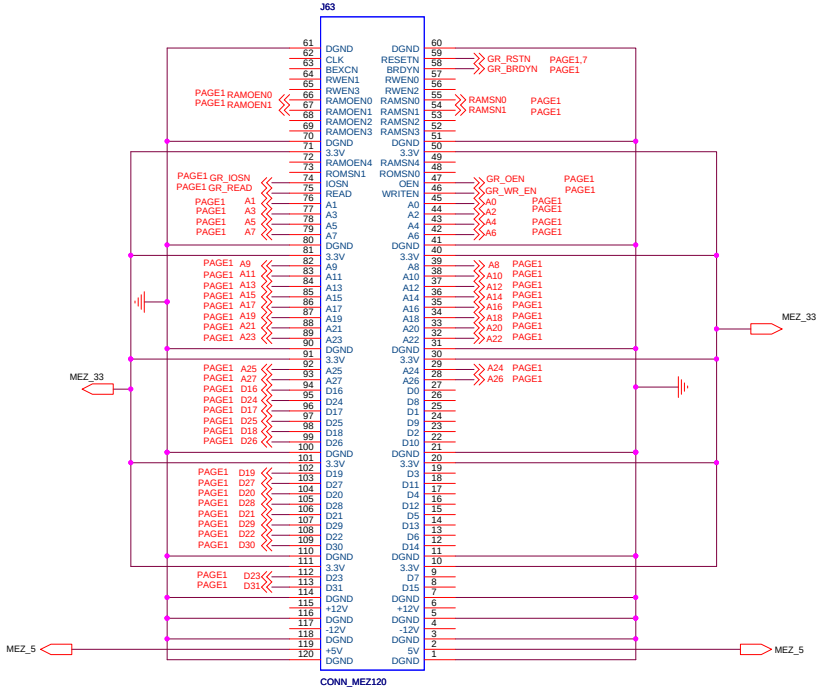
Size	CAGE Code	DWG NO	Rev
C	65342	ES4350222-001	-

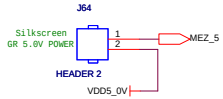
Tuesday, August 24, 2010 | Scale | Larsen | Sheet 4 of 7

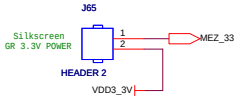


Aeroflex Colorado Springs 4350 Centennial Blvd. Colorado Springs Colorado 80907			
AEROFLEX	UT200SpW4RTR-EVB POWER		
	Size: C	CAGE Code: 65342	DWG NO: ES4350222-001 Rev: -
Tuesday, August 24, 2010	Scale	Larsen	Sheet: 5 of 7

Change Block







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UT200SpW4RTR-EVB GAISLER			
Size: C	CAGE Code: 65342	DWG NO: ES4350222-001	Rev: -
Tuesday, August 24, 2010	Scale:	Larsen	Sheet: 6 of 7

ORDERING INFORMATION

UT200SpW4RTR-EVB:

UT *****

Device Type:
200SpW4RTR-EVB = 4-port SpaceWire Evaluation Board

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi – Rel

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