What would happen to standard electronics if they were launched into space? From 500 to 75,000 km above the surface of the earth, space can be a very hostile environment to most electronics needed for such satellite functions as navigation, communication, and data processing.

The microprocessors, the high-density dynamic RAMs, and other vital electronics would operate for only a few months up to a year or two in many satellite systems before succumbing to the effects of radiation trapped in the earth's magnetic field [see following "The lowdown on ionizing radiation effects"]). During their relatively short life, the electronics could also suffer from bad data, spurious output signals, latch-up, or burn-out, all caused by the bombardment of galactic cosmic particles, of anything from hydrogen to uranium, that permeate the space above the earth.

Satellites have been around, of course. Defense, research, and geosynchronous communication satellites have been flying in these radiation belts for almost four decades. Radiation-hardened (rad-hard) electronics have been around, too. Electronics designed and built to operate effectively in a radiation environment have been in production for over 30 years. What is new is the need for rad-hard parts in quantities of tens or hundreds of thousands for commercial satellite systems at costs close to their unhardened commercial equivalents.

Rad-hard integrated circuits require special processing and, for the most part, have been manufactured on dedicated wafer fabrication lines. Because of the high cost of maintaining this kind of facility and the relatively small market for high-level rad-hard products, the cost of these components could easily exceed the cost of their commercial equivalents by a factor of 10 to 100.

For the military and such other applications as nuclear power and high-energy physics, which require small quantities of high-level rad-hard ICs, there is little choice but to buy products from the dedicated fab lines. But companies planning to put up communications satellites cannot afford the premium that rad-hard electronics have traditionally commanded.
The total dose. Over a 10-year mission in an outer-zone orbit, the total surface of the satellite and the electronics inside has a large effect on so, in the outer zone, the amount of shielding between the external surface of the satellite and the electronics inside has a large effect on the total dose. Over a 10-year mission in an outer-zone orbit, the total dose can range from much more than 1 Mrad(Si) for 1 g/cm² of shielding (about 3.7 mm of aluminum) to less than 10 krad(Si) if shielding is increased to 3 g/cm².

Economical hardening approaches
Unhardened commercial electronics can frequently survive 3-10 krad(Si) of total dose without much parametric degradation. They can also remain functional (although degraded) from 10-30 krad(Si), but they may suffer a high single-event upset rate or possible latch-up when struck by heavy ions. But because of the sensitivity of most commercial electronics to ionizing radiation, almost all satellite systems require some means of mitigating the system degradation due to space radiation.

The fabrication recipes used to harden ICs against total ionizing dose are closely guarded secrets, protected either by government or company classifications. What can be examined, though, are some particulars about the principal factors affecting the total dose tolerance.

The first step in hardening a CMOS IC against total dose radiation is to minimize voltage shifts or their impact in the circuit due to radiation-induced charge trapping in the gate and field oxides. Two approaches can be used, either individually or in parallel: reducing the number of holes trapped in the dielectric, and compensating for the trapped holes with trapped electrons.

The easiest way to minimize the trapped-hole density is to thin down the oxide. A clean gate oxide less than 12.5 nm thick, which is typical of today's commercial integrated circuits, can usually survive up to 100 krad(Si) with no process changes. Gate oxides on many current commercial ICs are as thin as 10 nm and the trend is toward even thinner oxides to maintain performance as operating voltages drop.

On the other hand, where local oxidation of silicon is used, field oxides must remain thick to meet isolation and planarity requirements. Minimizing the trapped-hole density in them is much trickier and requires special processing; for example, maintaining a smaller thermal budget. But it is also possible to eliminate the field oxide entirely through a fully depleted technology such as silicon-on-insulator.

As research over the past 20 years has shown, almost all IC process steps can either raise or lower the density of hole traps, the areas that will fill with holes when irradiated. This is why dedicated fabrication facilities are needed to produce ICs hardened to 1 Mrad(Si) or more. When rad-hard products are run on commercial lines using modified steps, it may be possible to reduce the hole traps — but in the absence of a dedicated rad-hard process, the hardness will rarely go much beyond 100 krad(Si).

Adding electron traps to offset the hole traps is another method of countering radiation effects on field or isolation oxide structures. Electron-trapping material (the details are proprietary) can be distributed throughout the field oxide or applied over its top. Then, as ionizing radiation produces electron-hole pairs and as the holes become trapped in the field oxide, electrons also become trapped, caught in the added electron traps, keeping the field or isolation oxide threshold voltages pinned. This approach can be used in combination with conventional processes in some commercial foundries with few changes to the underlying semiconductor processing. Hardness levels in excess of 100 krad(Si) can be achieved.

Radiation-hardened components fabricated on dedicated rad-hard lines are frequently hard to 1 Mrad(Si), and they can easily survive most natural space radiation environments.
Unfortunately, while this approach works in essentially all space environments, it is an expensive solution. But fortunately, since many satellite systems had only a few satellites and were government-funded, the premium paid for parts from dedicated rad-hard lines was not an important issue—until recently.

Now, with the current expansion of commercial satellite systems, some of which need more than 100 satellites in their constellation, a large market has arisen for innovative, lower-cost solutions to surviving and operating amid natural space radiation. That new market now offers several alternatives to dedicated rad-hard products.

One alternative, the self-contained process module, was introduced by UTMC, Colorado Springs, Colo., in 1997. This technique uses a commercial unhardened foundry for all IC process steps but adds a single series of processing operations as well. ICs are processed on the commercial line up to a certain point, segregated from the line for additional operations, and then merged back into the commercial line until they're completed. Recent data show that a total hardness level in excess of 100 krad(Si) has been achieved with this process. Single-event upset hardness and latch-up immunity, the equivalent of what is found in dedicated commercial radiation-hardened products, are obtained through design and through choice of a starting material such as thin-epitaxial silicon wafers.

This approach has several advantages: radiation hardness sufficient for most orbits at a cost a good deal lower than that of dedicated wafer fabrication facilities; higher levels of integration because of the use of advanced commercial design rules; and full control over the self-contained process steps. A disadvantage is that there is little control over the commercial portion of the fabrication process, which limits the ultimate radiation hardness achievable.

A similar approach is to produce radiation-hardened devices on the same line as commercial products by making adjustments to the commercial process or adding extra process steps throughout the flow. This technique has generally been successful in producing rad-hard devices up to about 100 krad(Si). The ultimate hardness of the product is usually limited to that level because only limited variations to the unhardened commercial flow are allowed, so as not to impact the cost or yield of the commercial products. As with the first approach, single-event-upset hardness and latch-up immunity, on a level with dedicated commercial radiation-hardened products, are obtained through design or starting material.

The plus side of this approach is generally lower product costs than possible with dedicated wafer fab facilities because of the ability to leverage capital equipment costs with the commercial markets. The down side is the difficulty convincing commercial semiconductor manufacturers to allow changes in their process flow.

Using radiation shields, typically of a tungsten/copper alloy, is another choice. They can either be built into the package structure or be attached to the top and bottom. While they are effective in reducing the electron component of the total dose radiation, they are much less effective in lessening the proton radiation. Ultimately, the hardness of the shielded but unhardened commercial component depends on the orbit. In low-to-medium earth-orbits of 1000 km to 7000 km, hardness may increase by a factor of only three—from 10 to 30 krad(Si), for example—and a 10-year mission could require components hardened to at least 100 krad(Si).

On the other hand, in high earth-orbits, such as a geosynchronous one, the effectiveness of shielding is quite high, usually increasing the total dose resistance by a factor of over 100. Of course, in the final analysis, the increase in hardness is simply related to the amount of shielding applied.

The main advantage of radiation
Radiation in space inflicts various single-event phenomena on semiconductor circuitry. The two that satellite designers worry about most are single-event upset and single-event latch-up. Both the effects can be caused by a single heavy ion (or, through secondary mechanisms, a single neutron) passing through a critical node in an IC. Heavy ions produce a dense track of electron-hole pairs, and if the charge deposited and ultimately collected as free electrons and holes is greater than the critical charge of a memory cell, a single-event upset can occur. The energy deposited by a heavy ion can also induce latch-up through a parasitic current path, such as an npnp chain.

The susceptibility of ICs to single-event upsets depends on the amount of critical charge required to “flip” a bit and the probability that a particle with a linear energy transfer (LET) large enough to deposit that critical charge will strike a sensitive node. The LET of a particle is related to the density of the charge track that it produces: a particle with a higher LET, such as iron, will create more electron-hole pairs per unit path length than one with a lower LET, such as carbon or helium.

As the features of ICs continue to shrink, cell capacitance gets smaller, too, making it more likely that particles with lower LET will give rise to upsets. The susceptibility of ICs to single-event upset is measured in the number of errors per bit that occur in an IC in one day. The satellite designer can either deal with the errors by using an error detection and correction technique or simply ignore the bad data.

The error rate of a particular device is a function of the LET threshold and the error cross section (which is related to the collection volume in a sensitive node). Many space-bound ICs have LET thresholds greater than 37 MeV-cm²/mg or so, which means that particles with LETs of less than 37 will cause few, if any, upsets. There is nothing magical about the number 37, but it is convenient for two reasons: it is achievable without making the storage cells too large and there are orders of magnitude more particles in space with LETs less than 37 than particles with LETs greater than 37.

Of course, it is error rate and not linear energy transfer threshold that is the important metric, and if (or rather, when) satellite designers begin demanding higher-density ICs, the LET threshold of ICs could decrease significantly. Although shrinking the physical dimensions generally means lower LET thresholds, it also (usually) means a lower error cross section, which helps to counteract that decrease in threshold.

The single-event upset problem is further complicated, however, if low-voltage devices are used, say, 3.3-V instead of 5-V components. In many applications, cell capacitance alone will be too little to deliver an acceptable upset rate; so other methods for minimizing single-event upset, such as error detection and correction and redundancy, will be required.

Single-event upsets are generally soft errors, which means that although the data in the upset cell is permanently lost, the cell can be still rewritten with new data with no change in its operating characteristics. Single-event latch-ups, on the other hand, can cause both a soft and a hard failure. The soft failure can be repaired by switching the power off and then back on. But latch-up may also cause parasitic currents large enough to burn out the junctions and permanently destroy the IC.

Much of the electronics considered for space use are required to be immune from latch-up to a LET of at least 90 MeV-cm²/mg. In contrast to single-event upset, hardening ICs against latch-up could actually get easier with advancing technology. Lower-voltage products are more resistant to latch-up than those with a higher voltage, and many of the silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) technologies are inherently immune to latch-up because there are no parasitic paths.

— J.M.B.
Electrons and protons become trapped in belts around the earth whose magnetic field constrains them to spiral around the field lines. The particles are reflected back and forth near the polar regions, where the field lines are more concentrated. Electrons and protons trapped in the field lines drift in opposite directions around the earth, giving rise to the radiation belts.

6000 km, where a good portion of the total dose is delivered by trapped protons, the total dose delivered and collected by ICs during a 10-year mission ranges from 50 to 2000 krad(Si)—too high for unshielded screened commercial parts to be used.

Shielded commercial parts may also be impractical at these elevations because thick and heavy shields would be required to protect unhardened components from total dose damage. The additional shield weight could become so great, in fact, that the cost of launching this extra weight could top US $1000 per IC.

What choices are left for satellite systems planned for 1000 and 1500 km above the earth? Full 1-Mrad(Si) hard dedicated components can fly in these orbits; but for commercial satellites their cost may be prohibitive. So far, the hardening techniques that are good enough to survive a 10-year mission, and also inexpensive enough to be competitive, are leveraged with commercial technology.
oxide and recombine with the trapped holes.) Many commercial IC gate oxides, with thicknesses generally of less than 12.5 nm, can easily survive greater than 100 krad(Si). So the hardness of commercial MOS ICs is usually limited by field-oxide degradation.

Ionizing radiation also boosts the interface trap density in MOS structures. Interface traps are localized electronic states close to the interface between silicon and silicon dioxide and can exchange charge with the silicon conduction and valence bands. They shift threshold voltage and can also degrade mobility by acting as scattering centers. They are an important issue for dedicated radiation-hard wafer fabrication lines where parts are qualified to more than 1 Mrad(Si). Nonetheless, because significant interface trap effects are seldom observed at total dose levels less than 100 krad(Si), they do not count for much for most radiation-tolerant ICs.

Although the primary area of research for radiation effects has been MOS structures, bipolar devices also exhibit some interesting total dose effects. Since silicon, unlike silicon dioxide, does not trap charges, it may at first appear that a total ionizing dose would hardly affect these minority-carrier devices. But state-of-the-art integrated bipolar technology contains isolation oxides. Charges trapped in these oxides can cause gain degradation at total dose levels as low as 10 krad(Si).

More bad news for space users of bipolar products was discovered in 1991, when data was reported that bipolar devices suffer from greater degradation when irradiated at the lower dose rates found in space, compared with rates used in the laboratory. This increased degradation was observed to be as large as a factor of five at dose rates below 1 rad(Si)/s, typical of the space environment, compared with common test and qualification dose rates between 50 and 300 rad(Si)/s.

Needless to say, low-dose-rate testing can be a heavy burden on the testing resources of chip vendors because of the additional time required to do the tests. —J.M.B.

As the commercial space business grows, it will no doubt drive the rad-hard market into more innovative and lower-cost solutions to the difficulties of hardening electronics. Hopefully, these rad-hard solutions will not only help to revolutionize global communications, but will also lower costs for more traditional rad-hard applications such as military, space, high-energy physics research, and nuclear power.

**To probe further**


**Single Event Phenomena** by G. C. Messenger and M. S. Ash (Chapman & Hall, New York, 1997) is recommended as a source for the basic physics involved.

Two excellent collections of single-event-upset research are the *IEEE Transactions on Nuclear Science* Special Issue on Single-Event Effects and the Space Radiation Environment (Vol. 43, April 1996) and the *IBM Journal of Research and Development* (Vol. 40, no.1, January 1996).

Annual meetings of the IEEE Nuclear and Space Radiation Effects Conference (NSREC) deal with research on radiation effects on devices and ICs, spacecraft environments, single-event phenomena, and hardness assurance techniques. The NSREC home page is: http://www.ieee.org/lpns/nsrec/snsrec.html.

NSREC papers can be found in December issues of the *IEEE Transactions on Nuclear Science* going back over 30 years. In particular, "Total dose effects in conventional bipolar transistors and linear integrated circuits," by A. Johnston and co-workers, describes the effects of total dose rate on device degradation (Vol. 41, 1994, p. 2427).

**About the author**

At the time of this writing, Joseph M. Benedetto was principal reliability engineer at UTMC Microelectronic Systems (now Aeroflex Microelectronic Solutions), Colorado Springs, Colo. He has investigated radiation effects on electronic devices for over 15 years. He also contributed to UTMC’s self-contained process module approach to radiation hardening ICs.

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